Powerex, Inc., 200 E. Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

1.0 Introduction

The small industrial inverter market is undergoing a trend toward system integration. There is a desire for better performance and more capabilities while at the same time decreasing the size and cost. This is a fundamental trade-off for integrated modules. The objective is to match the incorporated functions and package design to the application requirements to achieve the optimum system.

The ASIPM (Application Specific Intelligent Power Module) is a new power module technology targeted to simplify the design, enhance the performance, reduce the size and decrease the cost of small motor drives. The new Version 3 ASIPMs are designed for general-purpose industrial motor drive applications such as blowers, pumps, hoists, and conveyors. In these applications, the ASIPM provides a miniaturized power stage subsystem so that the motor drive can be simplified and more easily integrated into finished equipment.

The keys to Version 3 ASIPM technology are the integrated input rectifier, 6 IGBTs and FWDis, and an HVIC in a compact package for motor speed control. The HVIC has been specifically designed for these modules to provide gate drive and protection for all 6 IGBTs. The protection functions include control supply UV lockout, shoot-through interlock, short-circuit and overcurrent using a DC link current shunt. Added features include DC link analog current feedback signal, integrated bootstrap supply diodes, and fault signaling.

The new ASIPMs provide complete, compact power stage subsystems for a wide range of industrial motor drives. They dramatically reduce complexity and component count. Integrated control and protection features also help to increase reliability and significantly reduce development time. They are the key to miniaturization and cost reduction in these applications.

1.1 The Version 3 ASIPM Concept

Conventional IPMs (Figure 1.1), with integrated power devices and low voltage ASICs (Application Specific Integrated Circuits) to provide gate drive and protection functions, have been widely accepted for general purpose motor drive applications ranging from 200W to more than 150kW. The success of these modules is the direct result of advantages gained through increased integration. Some of these advantages include the following:

(1) Reduced design time and improved reliability offered by the factory tested, built-in gate drive and protection functions;

(2) Lower losses resulting from simultaneous optimization of power chips and protection functions;

(3) Smaller size resulting from the use of bare power chips and application specific control ICs;

(4) Improved manufacturability resulting from lower external component count.

Figure 1.1 Conventional IPM

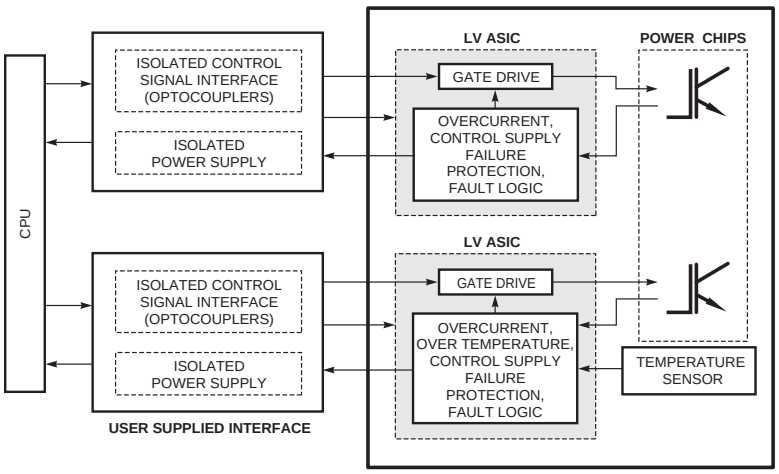
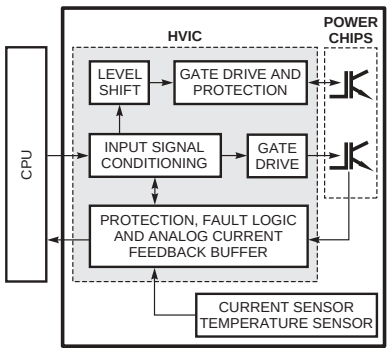


Figure 1.2 Version 3 ASIPM



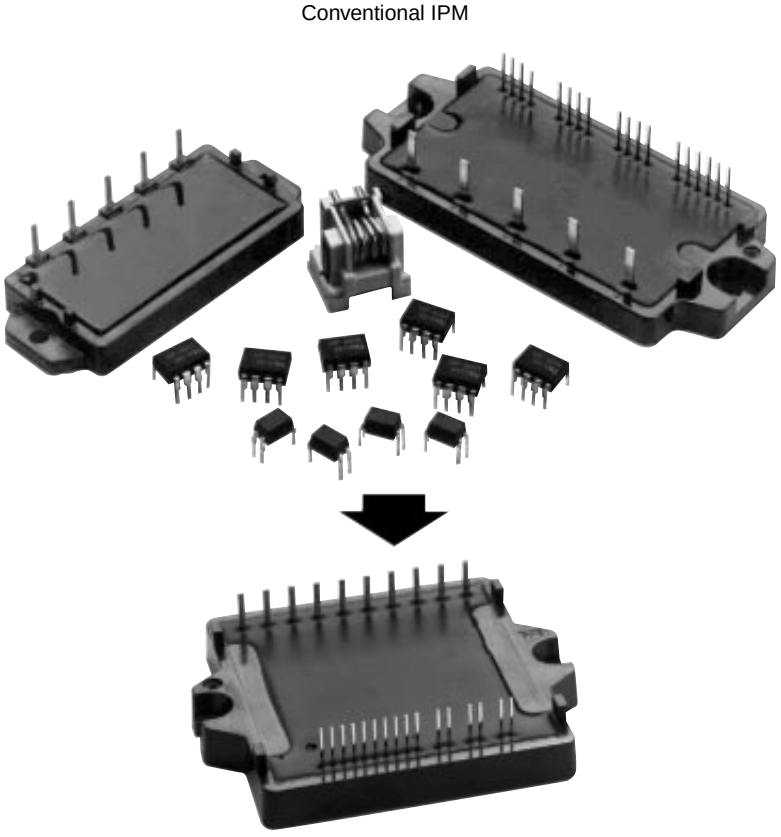
Unfortunately, in spite of these advantages, the conventional IPM's optically coupled interface circuit is often too expensive and complex to meet the demanding cost and size requirements of low-end industrial inverters. In most of these applications significant cost saving is obtained by utilizing HVICs to provide level shifting thereby eliminating the need for optocouplers. Additional savings are obtained by utilizing bootstrap power supplies for the high-side gate drivers rather than the four isolated supplies required by the conventional IPM.

The key to the Version 3 ASIPM, shown in Figure 1.2, is the integration of a custom HVIC to provide level shifting for the high-side IGBTs. This results in significant cost savings by allowing direct connection of all six IGBT control signals to the controller. The HVIC also provides gate drive and protection functions for both the high and low-side IGBTs. With just a few external components the entire three-phase power stage can operate from a single 15V control power supply. Incorporating the level shifting and bootstrap circuits into the Version 3 ASIPM reduces high voltage spacing requirements on the control PCB allowing a significant savings in circuit board space.

1.2 System Advantages

Figure 1.3 shows a comparison of the components required in a typical three-phase motor drive using a conventional IPM versus the Version 3 ASIPM. The Version 3 ASIPM replaces numerous external components. Clearly, there are significant manufacturing advantages to the Version 3 ASIPM approach. Incorporating the high-side power supplies and level shifting into the ASIPM helps to reduce the high voltage spacing requirements on the control PCB for a significant savings in circuit board space and reduced design time. The compact package of the Version 3 ASIPM combined with the smaller control board allows development of miniaturized inverters. The reduced manufacturing time and simplified assembly provided by the Version 3 ASIPM will allow improvements in both cost and reliability of the finished system.

Figure 1.3 Conventional IPM versus Version 3 ASIPM



2.0 Product Description

In order to address industrial motor drive applications operating on line voltages of 200VAC to 480VAC, the Version 3 ASIPMs were developed in two different voltage ratings, 600V and 1200V. The modules are available in a range of current ratings designed for inverters from about 200W to 3.7kW. Detailed line-ups and descriptions of the available Version 3 ASIPMs are provided in the following subsections.

2.1 Numbering System

(1) Device
PS1 = ASIPM

(2) Voltage (V_{CES})
1 = 600V
2 = 1200V

(3) ASIPM Version Number
03 = Version 3 ASIPM

(4) Nominal Inverter Rating
2 = 0.2 kW
3 = 0.4 kW
4 = 0.75 kW
5 = 1.5 kW
6 = 2.2 kW
7 = 3.7 kW (230V)
8 = 3.7 kW (460V)

Example:

PS1 1 03 6
(1) (2) (3) (4)

PS11036 is a Version 3 ASIPM with IGBTs rated at 600 Volts for a motor rating of 2.2 kW.

2.2 Line-up Tables and Typical Applications

The Version 3 ASIPM is a compact intelligent power module that integrates IGBTs and free-wheel diodes, along with gate drive and protection circuits. Table 2.1 lists the available Version 3 ASIPMs and summarizes the key characteristics and typical applications of each type.

Table 2.1 Version 3 ASIPM Line-up

Type	IGBT Ratings		Minimum	Included Functions		Typical Inverter Ratings**	
	V_{CES} (V)	I_C (A)	OC* Trip (A)	Thermistor	Rectifier	Output Current (I_O)	Motor
PS11032	600	4	4.3	No	Yes	1.5 ARMS	0.2kW, 230VAC
PS11033	600	8	8.5	No	Yes	3.0 ARMS	0.4kW, 230VAC
PS11034	600	15	14.2	No	Yes	5.0 ARMS	0.75kW, 230VAC
PS11035	600	20	19.8	No	Yes	7.0 ARMS	1.5kW, 230VAC
PS11036	600	30	31.1	No	Yes	11.0 ARMS	2.2kW, 230VAC
PS11037	600	50	86.7	No	No	17.0 ARMS	3.7kW, 230VAC
PS12032	1200	5	5.5	Yes	Yes	1.2 ARMS	0.2kW, 460VAC
PS12033	1200	5	7.6	Yes	Yes	1.8 ARMS	0.4kW, 460VAC
PS12034	1200	10	14.4	Yes	Yes	3.4 ARMS	0.75kW, 460VAC
PS12036	1200	15	23.3	Yes	Yes	5.5 ARMS	2.2kW, 460VAC
PS12038	1200	25	39.0	Yes	No	9.2 ARMS	3.7kW, 460VAC

*OC (Over Current) trip activates after 10μs delay
**Typical inverter rating based on 15kHz carrier frequency with 150% 60 sec overload requirement and $T_C \leq 100°C$, $T_j \leq 125°C$

2.3 Product Features

Figure 2.1 shows a basic block diagram of the Version 3 ASIPM integrated features. The key characteristics include:

Power Circuit:

- Three phase IGBT inverter bridge including six advanced 3rd generation IGBTs and six shallow diffused soft recovery optimized free-wheeling diodes.
- Three phase rectifier bridge for three-phase AC-to-DC power conversion. (Except PS11037 and PS12038)

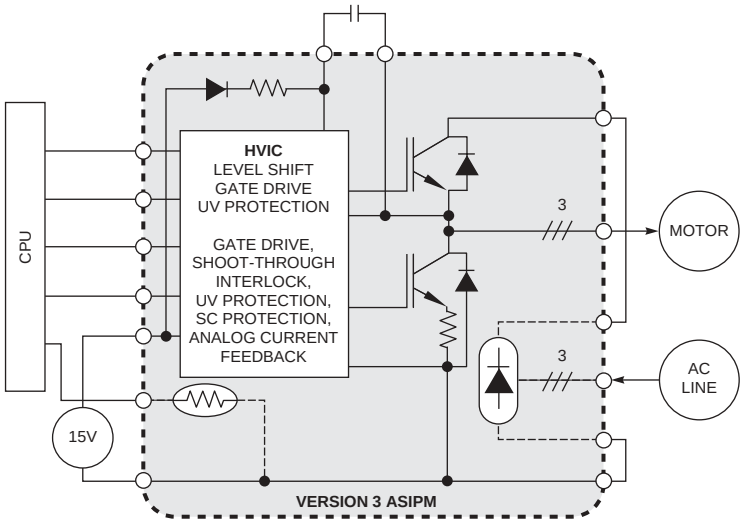
Control Functions:

- Built-in optimized gate driving circuits for all six IGBTs.
- 5V CMOS/TTL compatible control inputs with hysteresis for noise immunity.
- High voltage integrated circuit (HVIC) level shifters enable direct connection of all six IGBT gating control signals to the controller.
- Integrated bootstrap supply diodes allow operation from a single control power supply.
- DC link current analog feedback signal.
- Base plate temperature sensing with built-in thermistor. *In PS1203X types (1200V) only.
- Fault signaling for a SC or UV fault on the low-side IGBTs.

Protection Functions:

- N-side (low-side driver) control power supply undervoltage (UV) lockout.
- Short-circuit (SC) protection with soft shut-down using shunt in the negative DC-link.
- P-side (high-side driver) floating bootstrap supply undervoltage (UV) lockout.
- Shoot-through interlock protection.

Figure 2.1 Version 3 ASIPM Block Diagram

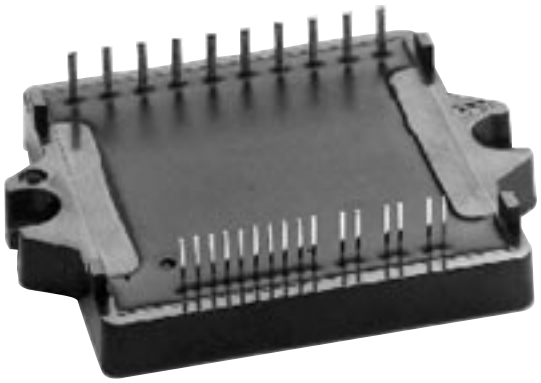


3.0 Packages

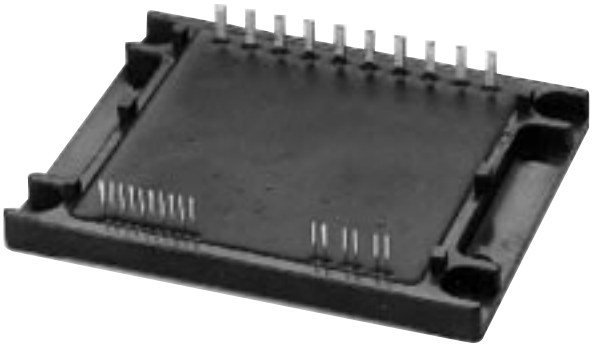
The Version 3 ASIPMs employ a low cost, rugged package optimized for small motor control applications. The packages are intended to reduce design time and simplify assembly.

There are five different package styles. The smallest package has two mounting bolts and the larger packages have four mounting bolts. The five packages are pictured in Figure 3.1. Detailed outline drawings with dimensions for each ASIPM can be found on the individual device data sheets. Descriptions of the control and power pin functions are in the following sections.

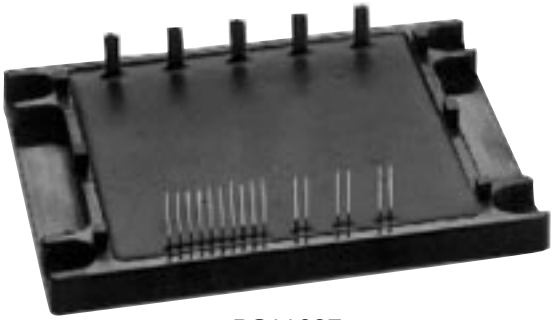
Figure 3.1 Package Photographs



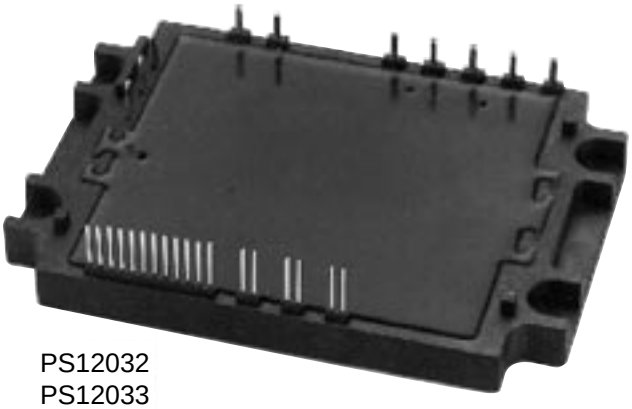
PS11032
PS11033
PS11034
PS11035



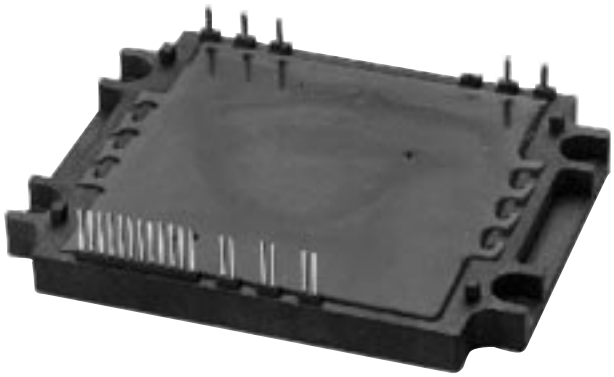
PS11036



PS11037



PS12032
PS12033
PS12034
PS12036



PS12038

3.1 Cross Section

A cross section diagram of the Version 3 ASIPM package is shown in Figure 3.2. The modules utilize a compact low profile IMS (Insulated Metal Substrate) package design. The figure shows a cross section of the IMS package with power chips, HVIC and support components assembled on the substrate. The single layer package technology has been optimized to allow a substantial reduction in inverter size.

The device is fabricated similar to a conventional surface mount printed circuit board. This process is easily automated, low cost and flexible. The IMS also provides an isolated aluminum base for direct mounting to a heat sink. The control and power pins are designed for direct soldering to a printed circuit board.

3.2 Terminal Description

Individual pin configurations are on each data sheet. Table 3.1 identifies the pin names and symbols and provides a detailed description of the pin functions. The terminal description is the same for both the PS1103X and the PS1203X series. However, not all pins are included on all modules. (Check the data sheets to see which pins are relevant.)

Figure 3.2 Cross Section of Version 3 ASIPM Package

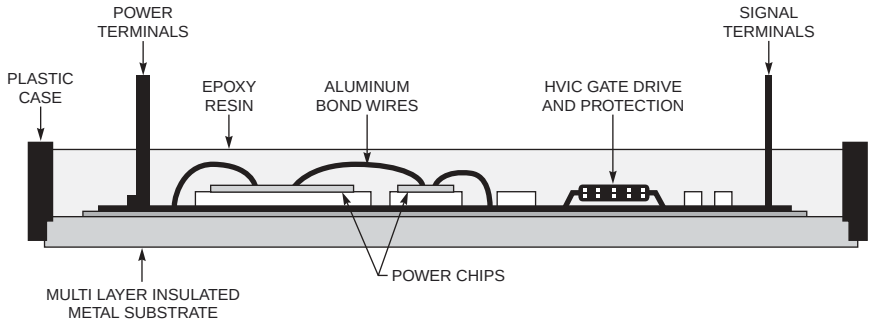


Table 3.1 Detailed Description of the Version 3 ASIPM Input and Output Terminals

Symbol	Name	Description
CBU±, CBV±, CBW±	Floating Supply Terminals	• These are the drive supply terminals for the P-side IGBTs. • No external power supplies are required for the ASIPM because of the integrated bootstrap circuits. • An electrolytic capacitor is connected to this terminal to provide the high-side floating power supply. (recommended value range: 2.2 ~ 22µF) • The bootstrap capacitor is charged from the N-side V_D supply during the ON-state of the corresponding N-IGBT in the loop. • Abnormal operation may result if the V_D supply is not properly filtered or has insufficient current capability. In order to prevent malfunction, this supply should be well filtered with a low impedance electrolytic capacitor and a good high frequency decoupling capacitor connected right at the ASIPMs pins.
GND	Ground Terminal	• This is the common signal ground point for the V_D control supply. • To avoid noise influences, current of the power circuit should not be allowed to flow through this terminal. • This terminal and N2 should not be connected externally by PCB patterns.

Table 3.1 Detailed Description of the Version 3 ASIPM Input and Output Terminals (continued)

Symbol	Name	Description
V_D	Control Supply Terminal	• This is the control supply terminal for the built-in HVIC protection functions and gate drive. • The ASIPM requires a 15V supply. Normally this supply is 15VDC ±10%. • In order to prevent malfunction caused by noise and ripple, this supply should be well filtered with a low impedance electrolytic capacitor and a good high frequency decoupling capacitor connected right at the ASIPMs pins. (electrolytic capacitor ≥33μF, film capacitor ~1μF) • To avoid potential malfunction of the control IC, the maximum ripple on the supply should be less than 2V peak-to-peak and the maximum dV/dt should be less than ±1V/ms.
U_P, V_P, W_P, U_N, V_N, W_N	Control Signal Terminals	• These are the input terminals for controlling the ASIPM switching operation. • Signals are active low 5V logic compatible. These terminals are internally connected to a Schmitt trigger circuit composed of 5V-class CMOS. • Built-in HVIC level shifting makes direct CPU connection possible without optocouplers. • Each signal line should be pulled up to plus side of the 5V logic power supply with approximately 5.1kΩ resistance. • The wiring of each input should be as short as possible (~2cm) to protect the ASIPM against noise. • A noise filtering capacitor should be connected to the 5V supply.
F_O	Fault Output Terminal	• This is the terminal for the fault output. A fault condition produces an active low output at this terminal (SC and UV operation at N-side). • This terminal is open collector type. The F_O signal line should be pulled up to plus side of the 5V power supply with approximately 5.1kΩ resistance. • Direct CPU connection is possible without optocouplers.
V_{amp}	DC Link Current Analog Feedback Signal Terminal	• Output from this terminal provides an analog voltage signal corresponding to the DC link current of the N-side IGBTs. • To prevent chances of signal oscillation, an RC filter at the output is recommended. • Direct CPU connection is possible without optocouplers.
R, S, T	Converter Input Terminals	• These are the power supply terminals to the front-end converter. • Line noise filter capacitors and surge absorbers between each input AC line and the power earth ground are recommended to improve noise immunity of the system.
P1	Converter Output Terminal	• This is the converter output terminal. • The inrush limiter should be connected between this terminal and P2.
P2	Inverter Input Terminal	• This is the power supply terminal to the inverter bridge. • It is internally connected to the collectors of the P-side IGBTs. • In order to suppress surge voltage caused by DC-link wiring or PCB pattern inductance, connect the main DC-link filter capacitors very close to the P2 and N2 terminals. It is also effective to add a film capacitor of good frequency characteristics. (0.1μF ~ 0.5μF)
N1	Converter Ground Terminal	• This is the power ground of the converter. • This terminal is connected to the negative side of the converter.
N2	Inverter Ground Terminal	• This is the power ground of the inverter. • This terminal is internally connected to the emitters of all lower-arm IGBTs and also to the control ground. The main power circuit current should flow through this terminal.
U, V, W	Power Output Terminals	• These are the inverter output terminals for connection to inverter load (AC motor). • Each terminal is internally connected to the center point of the corresponding IGBT half-bridge arm.
TH	Thermistor Terminal	• This terminal is connected to a thermistor mounted on the ASIPM's base plate. * This function is only available on the PS1203X series.

3.3 Installation Guidelines

When mounting a module to a heat sink, it is essential to avoid uneven mounting stress that may cause the device to be damaged or degraded. The mounting stress, heat sink flatness and thermal interface must, therefore, be considered carefully.

It is important to avoid uneven or excessive tightening stress. Figure 3.3 shows the recommended torque order for mounting screws. Use a torque wrench to tighten the screws. The maximum torque specifications are provided on each data sheet.

Mounting surface specifications are listed in Table 3.2. ASIPM base plate flatness is measured in both the X and Y directions as defined by Figure 3.4. The X and Y lines are drawn using the modules mounting holes as indicated. Heat sink flatness is measured as prescribed in Figure 3.5, which depicts the devices' footprint on the heat sink. The flatness of the heat sink underneath the module should be measured along the line shown in the figure. If the flatness of the heat sink is beyond the ranges, excessive uneven stress when installing a module to the heat sink might cause the device to be damaged or degraded.

The heat sink should have a surface finish of 64 micro inches or less. Use a uniform 4 to 8 mil coating of thermal interface compound. Select a compound that has stable characteristics over the whole operating temperature range and does not change its properties over the life of the equipment. See Table 3.3 for suggested types.

Figure 3.3 Recommended Torque Order for Mounting Screws

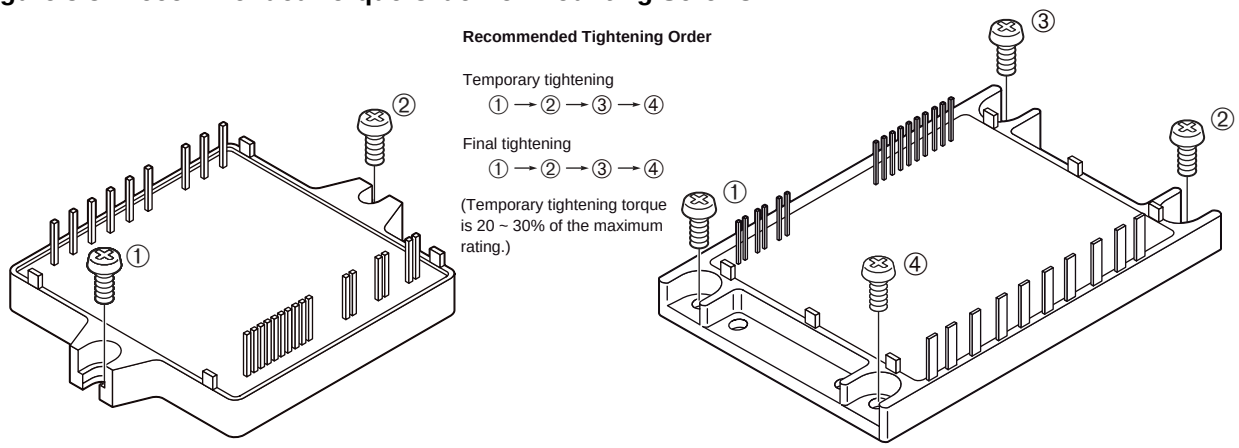


Table 3.2 Flatness Specifications

Type	Base Plate		Heat Sink		Units
	Minimum	Maximum	Minimum	Maximum	
PS11032	-50	+100	-100	+50	µm
PS11033	-50	+100	-100	+50	µm
PS11034	-50	+100	-100	+50	µm
PS11035	-50	+100	-100	+50	µm
PS11036	-50	+150	-150	+50	µm
PS11037	-50	+150	-150	+50	µm
PS12032	-50	+150	-150	+50	µm
PS12033	-50	+150	-150	+50	µm
PS12034	-50	+150	-150	+50	µm
PS12036	-50	+150	-150	+50	µm
PS12038	-50	+150	-150	+50	µm

Figure 3.4 Measurement Point for ASIPM Flatness

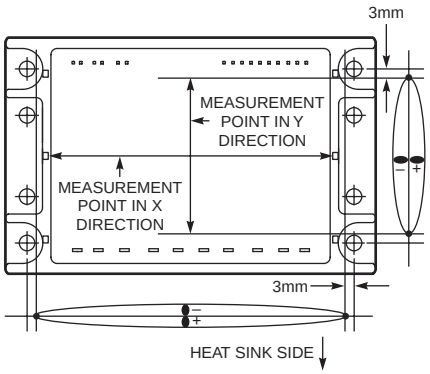


Figure 3.5 Measurement Point for Heat Sink Flatness

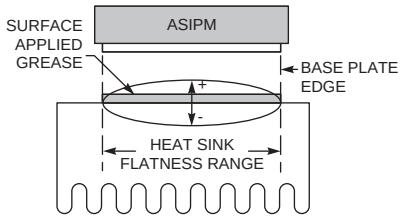


Table 3.3 Heat Sink Compounds

Manufacturer	Type
Shinetsu Silicon	G746
Dow Corning	DC340

4.0 Electrical Characteristics

The basic electrical characteristics and operation of the Version 3 ASIPM family are covered in this section. The protection functions and added features are presented here also. Detailed design information is presented in Section 5.

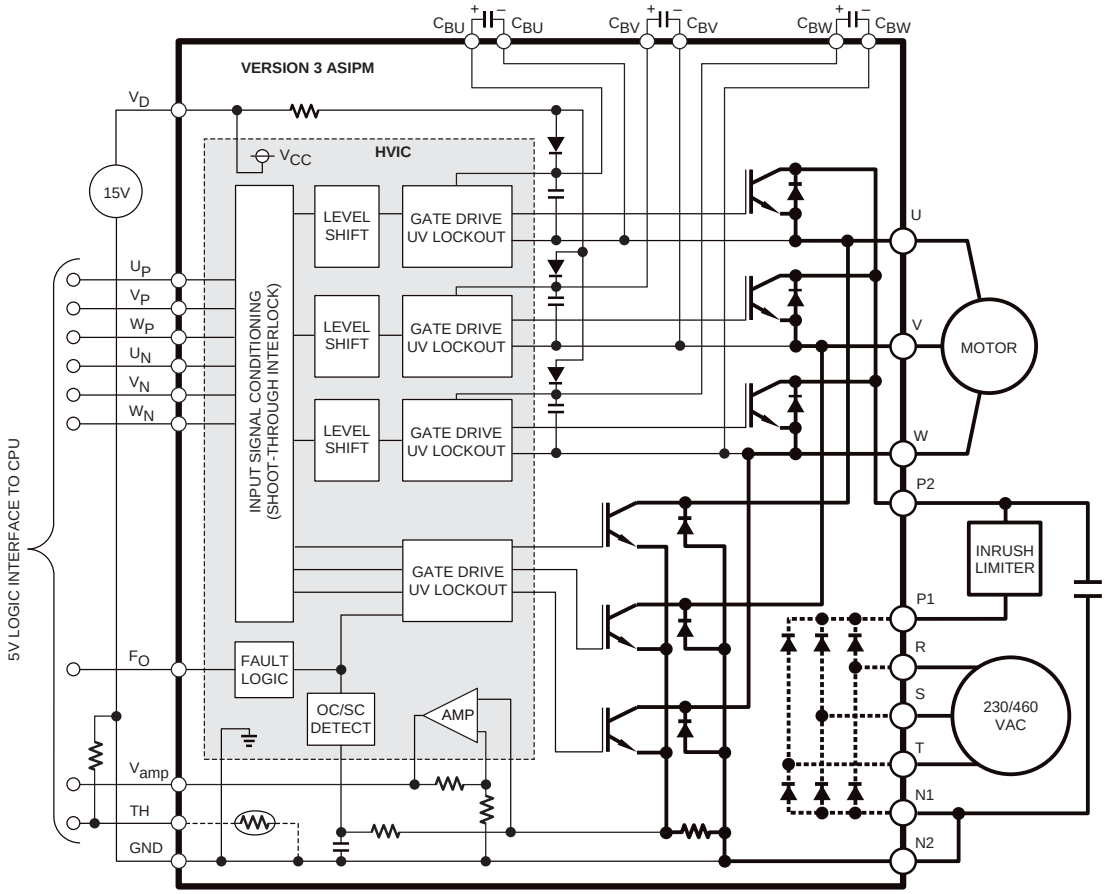
4.1 Functional Description

A functional diagram including a typical external circuit for the Version 3 ASIPM is shown in Figure 4.1. The internal components connected with dotted lines are not included in all types.

The power circuit of each device consists of six IGBT/free-wheel diode pairs configured as an inverter stage for a three-phase motor drive. All free-wheel diodes used in the Version 3 ASIPMs are super fast/soft recovery shallow diffused types. These diodes have been carefully optimized to have soft recovery characteristics over a wide range of currents in order to minimize EMI/RFI noise.

A single custom high voltage integrated circuit (HVIC) provides gate drive and protection functions for all six IGBTs. It is also employed to accomplish the level shift

Figure 4.1 Version 3 ASIPM Functional Diagram



for the high-side IGBTs. The result is a highly integrated power module that can be driven by a single drive power supply and directly connected to a CPU.

The ASIPM's built-in level shift eliminates the need for optocouplers and allows direct connection of all six control inputs to the CPU/DSP. The detailed operation and timing diagram for the level shift function is shown in Figure 4.2. The falling and rising edges of the P-side control signal (A) activate the one shot pulse logic which generates turn-on pulses (B, C) for the high voltage level shifting MOSFETs. Narrow ON pulses are used to minimize the power dissipation within the HVIC. The high voltage MOSFETs pull the input to the high-side driver latch (D, E) low to set and reset the gate drive for the P-side IGBT (F).

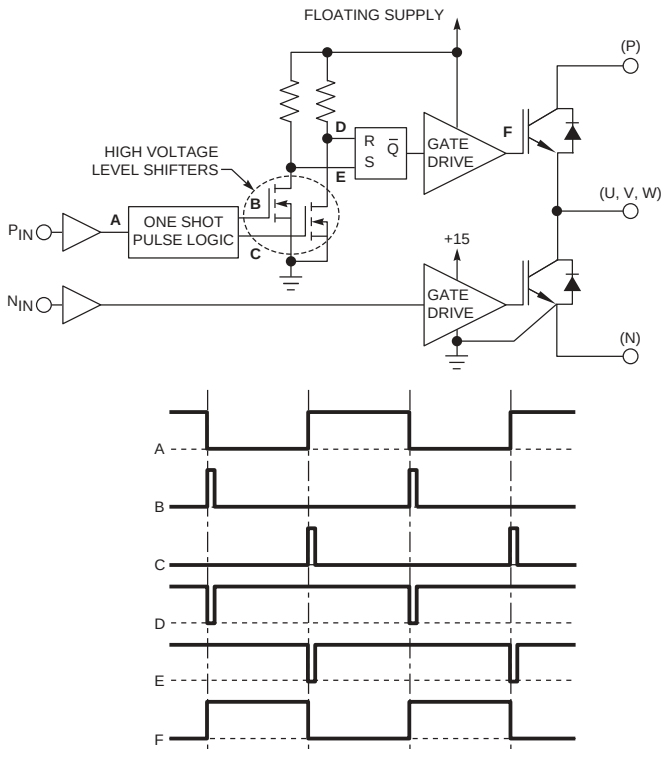
The integrated gate drive and protection functions provided by the HVIC are powered from a single external 15V control power supply referenced to the negative DC bus. Built-in bootstrap circuits supply floating power for the high-side gate drive circuits eliminating the need for separate isolated power supplies. External connections are provided to allow optimization of the bootstrap reservoir capacitors to meet the specific requirements of the application.

The Version 3 ASIPM is protected from failure of the 15V control power supply by a built-in undervoltage lockout circuit. If the voltage of the control supply falls below the UV level specified on the data sheet, the low-side IGBTs are turned off and a fault signal is asserted. In addition, the HVIC has independent undervoltage lockout circuits that protect the P-side IGBTs if the voltage of the bootstrap supplies becomes too low.

The Version 3 ASIPM has an integrated current shunt resistor in the negative DC bus. The voltage across the shunt is used to provide an analog current feedback signal as well as overcurrent and short-circuit protection. When an overcurrent or short-circuit condition is detected, the low-side IGBTs are turned off and a fault signal is generated.

The HVIC also provides shoot-through interlock logic to protect against noise and control signal anomalies. The interlock function rejects input signals that command the upper and lower IGBTs in a given leg to be on simultaneously. In addition to the functions described above, the 1200V Version 3 ASIPMs also include a built-in temperature sensor. The signal from the temperature sensor can be monitored by the system controller to provide over-temperature protection. All of these functions are discussed in detail later in Section 5 of this application note.

Figure 4.2 High Voltage Level Shift



4.2 Inverter Part

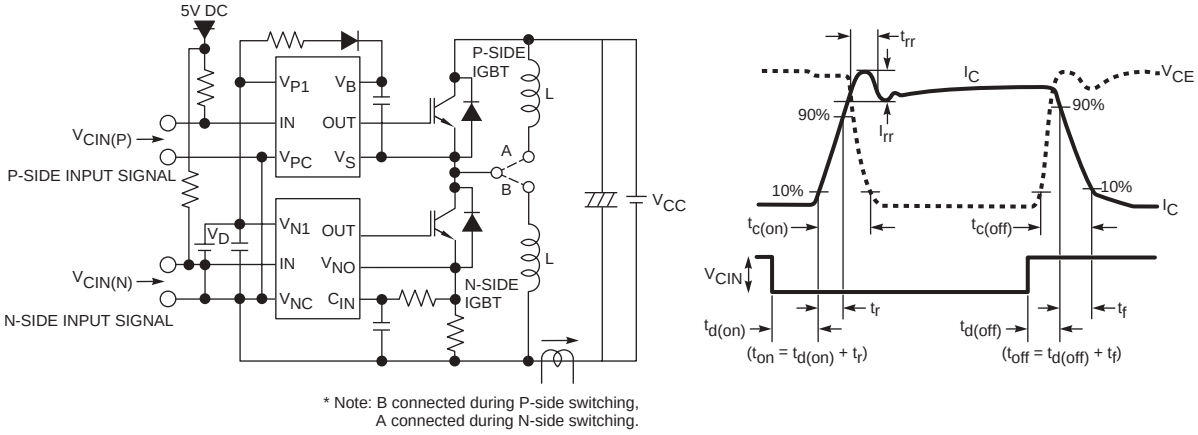
Table 4.1 lists the key static and dynamic characteristics for the inverter part of the Version 3 ASIPM. Example values (typical or maximum) are given for a 600V and a 1200V type.

The switching times given on the data sheets as electrical characteristics are for half-bridge inductive load. This reflects the fact that inductive loads are the most prevalent application for Version 3 ASIPMs. Figure 4.3 shows the standard half-bridge test circuit and switching waveform. The waveform illustrates how the data sheet parameters are defined.

Table 4.1 Electrical Characteristics of the Inverter Part

Symbol	Parameter	Conditions	PS11034	PS12034
V_{CES}	Collector-Emitter Voltage	Applied between P2-U·V·W, U·V·W·N2	600V	1200V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_D = 15V, V_{DB} = 15V, V_{CIN} = 0V, T_j = 25°C, I_C = 15A (The integrated resistor voltage drop is not included.)	2.9V	3.6V
$\pm I_C$ ($\pm I_{CP}$)	Collector Current (Peak Collector Current)	T_C = 25°C	±15A (±30A)	±10A (±20A)
V_{EC}	Diode Forward Voltage	V_{CIN} = 0V, T_j = 25°C, I_C = 15A	2.9V	2.9V
t_{on}/t_{off}	Switching Times	Inductive Load, V_{CIN} = 0V, V_{CC} = 300V,	0.6µs/1.6µs	1.2µs/2.2µs
$t_{c(on)}/t_{c(off)}$		I_C = 15A, T_j = 125°C, V_D = 15V, V_{DB} = 15V	0.5µs/0.5µs	0.5µs/0.9µs

Figure 4.3 Half-bridge Evaluation Circuit Diagram (Inductive Load)



4.3 Converter Part

Table 4.2 lists the most important characteristics for the converter part of the ASIPM. The same example types are used.

4.4 Control Part

The characteristics of the built-in control and protection functions are given in Table 4.3.

5.0 Application Guidelines

The Version 3 ASIPMs are based on advanced low loss IGBT and free-wheel diode technologies. The application issues and general guidelines are essentially the same for all of the Version 3 ASIPMs even though they have different combinations of functions. The information presented in this section is intended to help users of Version 3 ASIPMs apply the devices effectively and reliably.

5.1 System Connection Diagram

Figure 5.1 shows a typical system connection diagram for the Version 3 ASIPM. Component selection information and relevant notes are included below the figure.

Table 4.2 Electrical Characteristics of the Converter Part

Symbol	Parameter	Conditions	PS11034	PS12034
V_{RRM}	Repetitive Peak Reverse Voltage	Applied between P1-R·S·T, R·S·T·N1	800V	1600V
V_{FR}	Converter Diode Voltage	T_j = 25°C, I_{FR} = A	1.5V @ 10A	1.7V @ 12A
I_{DC}	DC Output Current	3-phase Rectifying Circuit	15A	12A

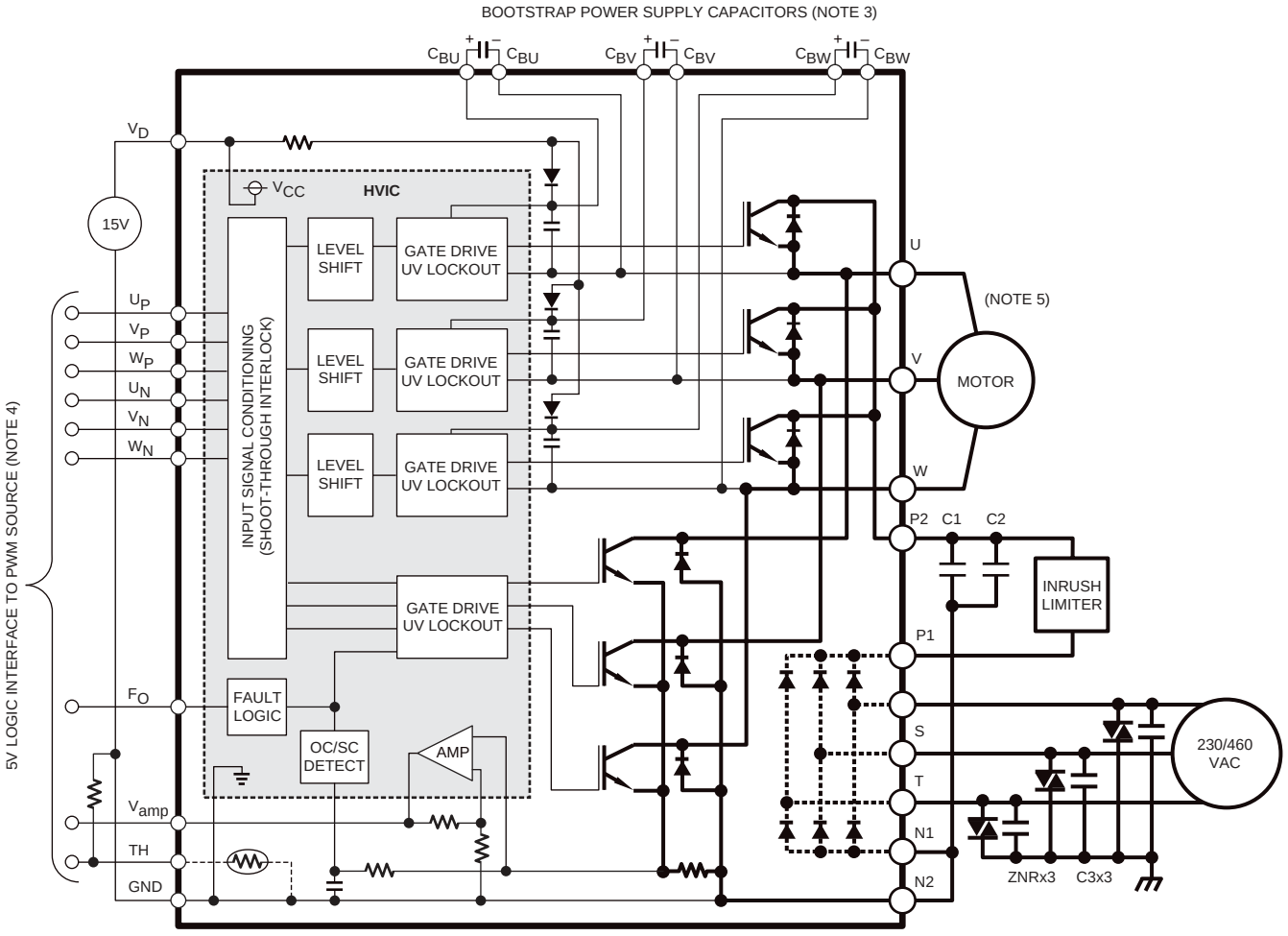
Table 4.3 Electrical Characteristics of the Control Part

Symbol	Parameter	Conditions	PS11034	PS12034
t_{int}	Input Interlock Sensing Time	(Relates to corresponding input signal for blocking arm shoot through.)	100ns	100ns
$V_{amp(100\%)}$	DC Link Current Analog Feedback Signal	I_C = $I_{OP(100\%)}$*, V_D = 15V, T_C = 25°C	2.0V	2.0V
$V_{amp(200\%)}$		I_C = $I_{OP(200\%)}$*, V_D = 15V, T_C = 25°C	4.0V	4.0V
OC	Overcurrent Protection Trip Level	T_j = 25°C	17.7A	17.2A
t_{OC}	Overcurrent Protection Filter Time	T_j = 25°C	10µs	10µs
SC	Short-circuit Protection Trip Level	T_j = 25°C	30A	25.8A
t_{SC}	Short-circuit Protection Filter Time	T_j = 25°C	2µs	2µs
UV_D	Supply Circuit Undervoltage Protection	Trip Level, T_C = 25°C	12.0V	12.0V
UV_{Dr}		Reset Level, T_C = 25°C	12.5V	12.5V
UV_{DB}		Trip Level, T_C = 25°C	10.8V	10.8V
UV_{DBr}		Reset Level, T_C = 25°C	11.3V	11.3V
t_{dv}	UV Delay Time	T_C = 25°C	10µs	10µs
t_{FO}	Fault Output Pulse Width	T_j = 25°C	1.8ms	1.8ms
R_{TO}	Thermistor Resistance	T_O = 25°C (298K)	NA	10kΩ
β	Material Constant	T_1 = 25°C, T_2 = 50°C**	NA	3450K

*I_{OP} = I_O • √2 where I_O is from Table 2.1 in Section 2.2

**$$T = \frac{1}{\frac{1}{\beta} \bullet \ln\left[\frac{R_T}{R_{TO}}\right] + \frac{1}{T_O}}$$

Figure 5.1 Version 3 ASIPM System Connection Diagram



Component Selection:

Dsgn.	Typ. Value	Description
C1	200-2000uF, 450V	Main DC bus filter capacitor – Electrolytic, long life, high ripple current, 105°C
	or 100-1000uF, 900V	Use two 450V capacitors in series for 460VAC applications
C2	0.1-0.22uF, 450V	Surge voltage suppression capacitor – Polyester/Polypropylene film (Note 1)
	or 0.1-0.22uF, 900V	Use 900V for 460VAC applications
C3	2.2-6.5nF	Common mode noise suppression filter – Polyester/Polypropylene film (Note 2)
ZNR	Line Voltage	Transient Voltage Suppressor – MOV (Metal Oxide Varistor)

Notes:

1) The length of the DC link wiring between C1, C2 and the ASIPM's P2 and N terminal must be minimized to prevent excessive transient voltages. In particular, C2 should be mounted as close to the ASIPM as possible.
2) Common mode noise (dV/dt) suppression capacitors are recommended to prevent malfunction of ASIPM's internal circuits.
3) Bootstrap capacitors provide floating power supplies for high-side gate drivers. Component values must be adjusted depending on the PWM frequency and technique. See text and interface circuit diagrams for details.
4) 5V logic level control signal interface to PWM controller. See interface circuit diagram and text for details.
5) If there is a possibility of high dV/dt noise at the inverter output (i.e. mechanical contactor, etc.) an output filter should be used.

5.2 Control Power Supplies Design

In most applications the Version 3 ASIPM will use a single 15V control power supply to power the built-in gate drive, level shifting and protection functions. The main 15V source (V_D) supplies power directly to the low-side IGBT gate drivers and protection circuits. The common reference of the V_D supply is at the negative DC bus potential. This is also the common reference for all of the logic level control input signals. Normally a 5V logic power supply with the same common reference is required to provide pull-up for the control input signals. This power supply is often used to provide power for the PWM controller as well. Three floating 15V power supplies (V_{DB}) for the high-side gate drivers are developed using built-in bootstrap circuits. The following subsections describe the detailed operation and timing requirements for all of these control power supplies.

5.2.1 Main Control Power Supply

Control and gate drive power for the ASIPM is normally provided by a single 15VDC supply that is connected at the modules V_D and GND terminals. For proper operation this voltage should be regulated to 15V ±10%. Table 5.1 describes the behavior of the ASIPM for various control supply voltages. This control supply should be well filtered with a low impedance electrolytic capacitor connected right at the ASIPM's pins. High frequency noise on the supply may cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than 2V peak-to-peak and the maximum dV/dt should be less than ±1V/µs. It is very important that the control power supply is connected to the GND terminal and not to the N2 terminal. The N2 and GND terminals are connected inside the ASIPM. These terminals should never be connected together externally. If these terminals are connected current flowing through the ground loop may cause the ASIPM to malfunction. In general, it is best practice to make the common reference at GND a ground plane in the printed circuit layout.

The main control power supply is also connected to built-in bootstrap circuits that are used to establish the floating supplies for the high-side gate drivers. The bootstrap supply operation will be discussed in more detail in Sections 5.2.4 through 5.2.7.

5.2.2 The 5V Logic Power Supply

The ASIPM's active low control inputs require 5V logic level signals to provide ON and OFF commands for the six internal IGBTs. The configuration of these inputs is described in more detail in Section 5.3.1. The inputs are not suitable for operation at 15V. A 5V logic power supply referenced to the same common as the main control power supply is required to provide pull-up for these inputs. In applications where the inputs are directly connected to the controller the 5V supply is also used to power the controller.

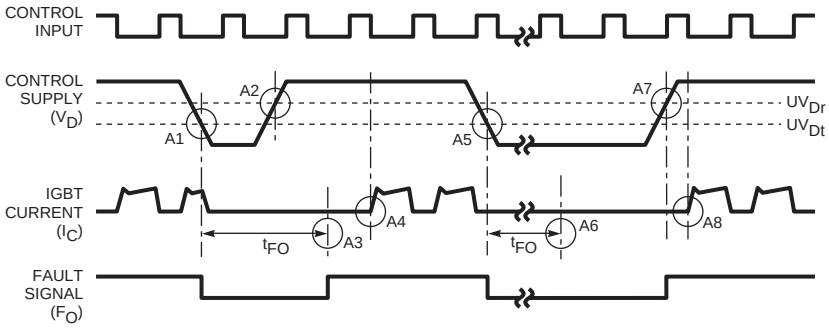
Table 5.1 ASIPM Functions versus Control Power Supply Voltage

Main Control Power Supply Voltage (V_D)	ASIPM State
0V ~ 4V	Control IC does not function. Undervoltage lockout and fault output do not operate. dv/dt noise on the main P-N supply may trigger the IGBTs.
4.0V ~ 12.5V	Control IC starts to function. Undervoltage lockout activates, control input signals are blocked and a fault signal is generated.
12.5V ~ 13.5V	Undervoltage lockout is reset. IGBTs will turn on when control inputs are pulled low. Driving voltage is below the recommended range so $V_{CE(sat)}$ and switching losses will be larger than normal.
13.5V ~ 16.5V	**Normal Operation. This is the recommended operating range.**
16.5V ~ 20V	IGBT switching remains enabled. Driving voltage is above the recommended range. Faster switching of the IGBTs will cause increased system noise. Peak short-circuit current may be too large for proper operation of the overcurrent protection.
20V+	Control circuit in ASIPM may be damaged.

5.2.3 Main Control Power Supply Undervoltage Lockout

The Version 3 ASIPM has an undervoltage lockout function to protect the IGBTs from insufficient driving voltage if the main control power supply voltage (V_D) becomes too low. If the voltage of the control supply falls below the UV_D level specified on the ASIPM's data sheet, for a period longer than t_{dV} (10µs typ.) the low-side IGBTs are turned off and a fault signal is asserted. The undervoltage lockout includes hysteresis to prevent oscillation. In order to clear the fault V_D must exceed the undervoltage reset level UV_{Dr} specified on the data sheet and the fault timer (t_{FO}) must expire. The fault signal will be cleared and normal operation will resume on the first high to low transition (turn-on) of the control signal after the control voltage exceeds the under voltage reset level (UV_{Dr}). Figure 5.2 shows the timing diagram for the main control power supply under voltage protection function. Figures 5.3 and 5.4 show the typical temperature dependence of the undervoltage trip level (UV_D) for 600V and 1200V Version 3 ASIPMs.

Figure 5.2 Main Control Power Supply (V_D) Undervoltage Lockout Timing Diagram



A1: Control supply falls below UV_D level. IGBT switching is stopped. Fault signal is asserted.
A2: Control supply exceeds UV_{Dr} level but no action is initiated because t_{FO} has not expired.
A3: t_{FO} timer expires and the fault signal is cleared.
A4: Switching of IGBT resumes at the first ON transition after the fault signal is cleared.
A5: Control supply falls below UV_D level. IGBT switching is stopped. Fault signal is asserted.
A6: t_{FO} timer expires but no action is initiated because the control supply is still below the UV_{Dr} level.
A7: The control supply exceeds the UV_{Dr} level and the fault signal is cleared.
A8: Switching of the IGBT resumes at the first ON transition after the fault signal is cleared.

Figure 5.3 Temperature Characteristics of Control Supply Undervoltage Lockout for PS1103X

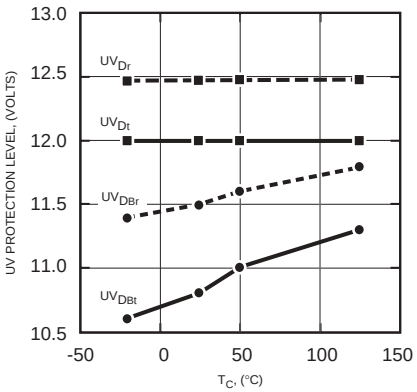
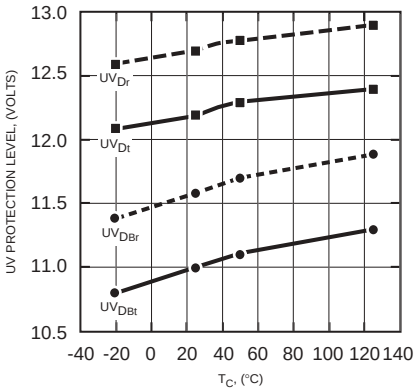


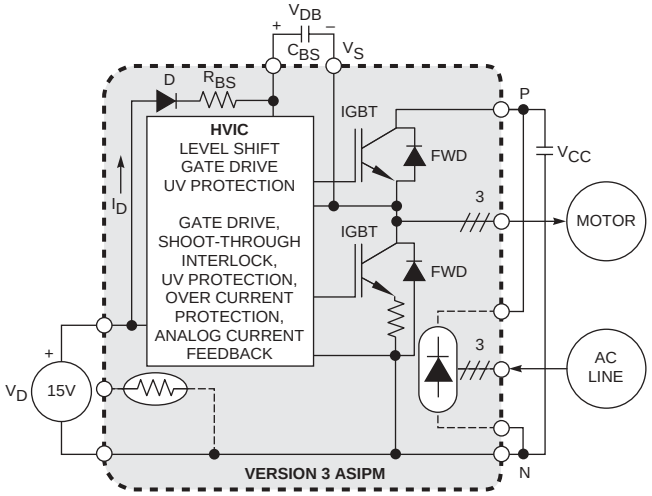
Figure 5.4 Temperature Characteristics of Control Supply Undervoltage Lockout for PS1203X



5.2.4 Bootstrap Power Supply

In most applications the Version 3 ASIPM's will generate floating power supplies for the high-side gate drivers from the main control power supply using built-in bootstrap circuits. A typical bootstrap circuit is shown in Figure 5.5. When the low-side IGBT (IGBT2) is turned on, current flows from the low-side control power supply (V_D) through the diode D and inrush-limiting resistor R_{BS} to charge the high-side reservoir capacitor (C_{BS}). C_{BS} then supplies power for the high-side gate drive while IGBT2 is off. The inrush-limiting resistor (R_{BS}) is included to prevent the bootstrap charging current pulses from producing excessive ripple on the control power supply. The bootstrap diode D blocks the full DC bus voltage when IGBT2 is off. The bootstrap supply reservoir capacitor must be sized so that sufficient voltage is maintained on the high-side gate driver during the off time of IGBT2. Some guidelines for selecting this capacitor will be provided in the following sections. Using this technique it is possible to operate all six IGBT gate drivers from a single 15V supply. The bootstrap circuit is a very low cost method of providing power for the high-side IGBT gate drive. However, care must be exercised to maintain the high-side supplies when the inverter is idle and during fault handling conditions. This usually means that the low-side IGBTs must be pulsed on periodically even when the inverter is not running. At power-up, the boot strap supplies must be charged before the PWM is started. Normally, this is accomplished by applying a train of short pulses to the low-side IGBTs until the bootstrap capacitors are fully charged.

Figure 5.5 Bootstrap Circuit



5.2.5 Bootstrap Power Supply Timing Diagrams

There are two conditions under which the bootstrap reservoir capacitor will charge. The first condition (Case 1) is when the low-side IGBT (IGBT 2) is on. When IGBT2 first turns on the voltage on CBS (VDB) is given by:

$$V_{DB(1)} = V_D - V_F - V_{CE(sat)2} - i_D \times R_{BS} \quad \text{(Dynamic Condition)}$$

where:

$V_{DB(1)}$ = bootstrap supply voltage (Case 1)

V_D = main control supply voltage

V_F = forward voltage drop across D at i_D

$V_{CE(sat)2}$ = saturation voltage of IGBT2

i_D = bootstrap supply charging current

R_{BS} = bootstrap resistor

As the voltage on the bootstrap reservoir capacitor increases the charging current decreases and the steady state voltage V_{DB} becomes nearly equal to the main control supply voltage V_D.

$$V_{DB} = V_D \text{ (Steady State)}$$

When IGBT2 is first turned off there will be a dead time during which neither IGBT1 or IGBT2 is on. The inductive load (motor) will force forward current through FWD1 bringing the voltage at V_S to nearly the positive DC bus voltage (V_{CC}). The bootstrap diode D becomes reverse biased cutting off the flow of bootstrap charging current (i_D). This sequence of events is shown in the timing diagram Figure 5.6. During the ON time of IGBT1 the bootstrap supply voltage (V_{DB}) gradually declines as the current consumed in the HVIC gate drive circuit discharges the reservoir capacitor.

The second condition under which the bootstrap supply capacitor will charge is when FWD2 is conducting (Case 2). This mode is illustrated in the timing diagram show in Figure 5.7. In this case IGBT1 is being turned on and off while IGBT2 is always off. During the time when both IGBT1 and IGBT2 are off the inductive load (motor) current will circulate through FWD2. When this happens the voltage at V_S becomes nearly equal to the negative bus voltage and D becomes forward biased allowing bootstrap charging current i_D to flow from the main control power supply. The i_D will begin recharging the bootstrap supply reservoir capacitor C. For this case the bootstrap supply voltage (V_{DB}) is given by:

$$V_{DB} = V_D - V_F + V_{EC2}$$

where:

V_{DB} = bootstrap supply voltage (Case 2)

V_D = main control supply voltage

V_F = forward voltage drop across D at i_D

V_{EC2} = forward voltage drop across FWD2

When IGBT1 is on the voltage at V_S becomes nearly equal to the positive DC-link voltage thereby reverse biasing D and stopping the flow of charging current (i_D). The bootstrap supply voltage (V_{DB}) then begins to gradually decline as the current consumed by the HVIC gate drive circuit discharges the reservoir capacitor.

Figure 5.6 Bootstrap Supply Charging (Case 1)

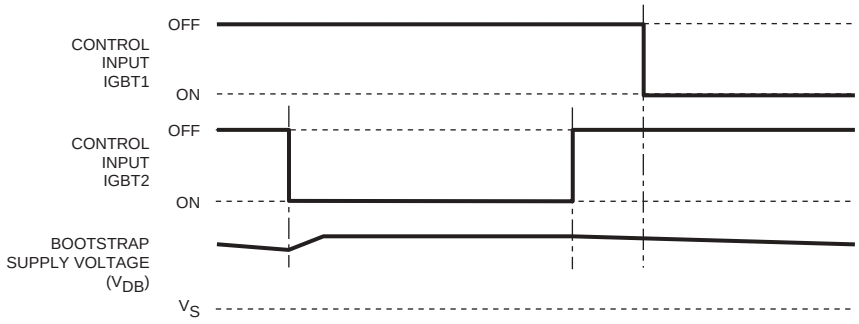
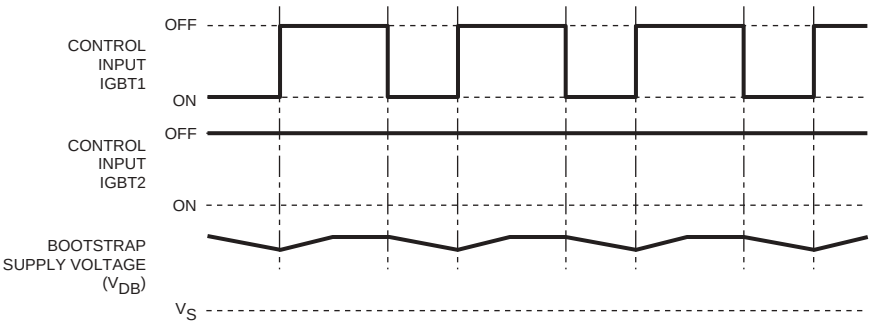


Figure 5.7 Bootstrap Supply Charging (Case 2)



5.2.6 Approximate Calculation for the Bootstrap Capacitor

The required bootstrap capacitance for an inverter system will depend on the detailed operating conditions including the PWM pattern, switching frequency, output frequency and drive-supply voltage. In addition, start-up, shut-down and fault sequences need to be considered. The following calculation is intended to provide a rough estimate of the required bootstrap capacitance in a typical sinusoidal output inverter. In order to simplify the computation some assumptions have been made that may not be true in a particular application. Therefore this calculation should be used only to provide approximate design values for the bootstrap capacitance.

Assumptions:

(i) Ordinary PWM pattern is used where the N-side IGBT is on whenever the P-side IGBT is off (except for the dead-time interval).

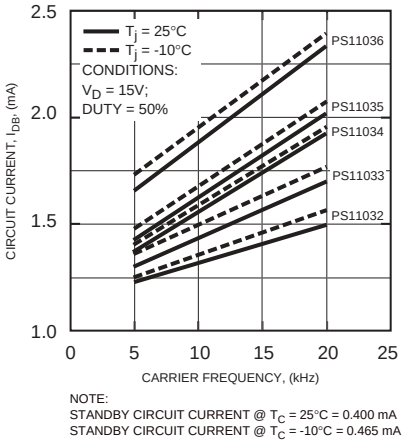
(ii) Maximum discharge of the bootstrap capacitor occurs during the period of the positive half-cycle of the output current waveform. This is generally true because the lower IGBT ON time is minimum and therefore there is less charging time for the bootstrap capacitor.

(iii) P-side IGBT circuit-current (i_{DB}) including the standby current of the HVIC at a given switching frequency is given by the experimental data taken at

a fixed 50% duty shown in Figures 5.8 and 5.9.

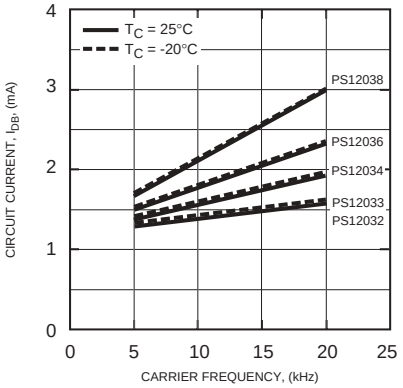
(iv) Drive-supply voltage = 15V, Case temperature = 25°C.

Figure 5.8 Typical Circuit Current of PS1103X Series versus Carrier Frequency



NOTE:
STANDBY CIRCUIT CURRENT @ T_C = 25°C = 0.400 mA
STANDBY CIRCUIT CURRENT @ T_C = -10°C = 0.465 mA

Figure 5.9 Typical Circuit Current of PS1203X Series versus Carrier Frequency



NOTE:
STANDBY CIRCUIT CURRENT @ T_C = 25°C = 0.435 mA
STANDBY CIRCUIT CURRENT @ T_C = -20°C = 0.466 mA

Simplified calculation expression:

Maximum capacitor discharge (Q_{max}) = (P-side IGBT circuit-current (I_{DB})) x (Output-current period/2)

or: $Q_{max} = I_{DB} \times (T_O/2)$

Approximate bootstrap capacitor value C_1 = maximum capacitor discharge (Q_{max})/(maximum voltage-drop across the capacitor (dV_{max}))

or: $C_1 = Q_{max}/dV_{max}$

Calculation example:

For an application using the ASIPM PS11034 (15A / 600V) at the following conditions:

Switching frequency = 15kHz,

Output Frequency = 60Hz = $1/T_O$,

Maximum allowable voltage-drop across the bootstrap capacitor (dV_{max}) is 1V

Referring to the P-side IGBT drive current (I_{DB}) data shown in Figure 5.8, at f_{SW} = 15kHz we get I_{DB} = 1.75 mA.

Then Q_{max} = 1.75mA x (16.67ms/2) = 14.6µC

And $C_{BS} = Q_{max}/dV_{max}$ = 14.6µC/1V = 14.6µF.

As noted above this calculated value of C1 should be used as an approximation only. The final design value should be determined after evaluating the performance of the bootstrap capacitor in prototype circuits applying the actual PWM pattern and considering all inverter operating modes.

NOTE: The bootstrap current limiting resistor (R) integrated within the ASIPM is 8.2Ω for the PS1103X series.

5.2.7 Bootstrap Supply Undervoltage Lockout

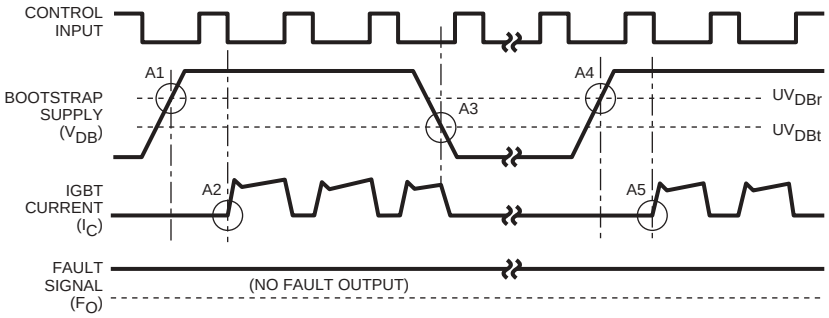
The HVIC driver in the Version 3 ASIPM provides an undervoltage lockout function to protect the high-side IGBTs from insufficient gate driving voltage. If the voltage on any of the bootstrap power supplies drops below the data sheet specified undervoltage trip level (UV_{DB}) for longer than t_{dV} the respective high-side IGBT will be turned off and input control signals will be ignored. The t_{dV} delay, which is typically 10µs, is implemented to avoid nuisance tripping. In order to prevent oscillation of the undervoltage protection function, hysteresis has been provided. For normal operation to resume, the bootstrap supply voltage must exceed the data sheet specified undervoltage reset level (UV_{DBr}). Switching will resume at the next ON command after the supply has reached UV_{DBr}. A timing diagram showing the operation of the undervoltage lockout is shown in Figure 5.10. Note that the bootstrap undervoltage protection function does not provide a fault signal.

5.2.8 Power Supply Start-up and Shut-down Sequence

Figure 5.11 depicts the recommended start-up and shut-down sequence of the control and logic power supplies. At start-up the logic power supply should exceed the input off threshold voltage before the control power supply reaches the undervoltage reset level as shown. At shut-down the control power supply should reach the undervoltage trip level before the logic power supply reaches the input ON threshold voltage.

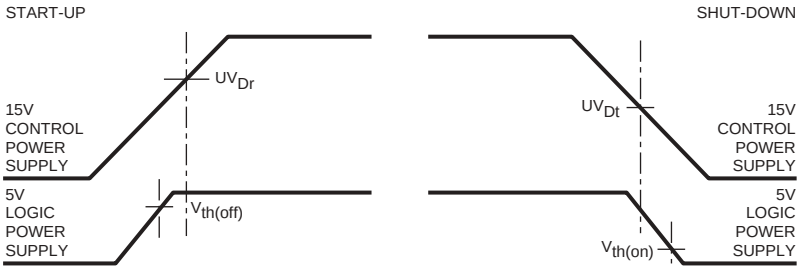
The concept is similar for the start-up and shut-down sequence of the control power supply and the main (P to N) power supply. The control power supply should be on and stable prior to the turn-on of the main supply. And, the main supply voltage should be removed before the control power supply is shut down. The above power supply sequences should be followed to ensure that the Version 3 ASIPMs do not malfunction.

Figure 5.10 Bootstrap Supply Undervoltage Lockout Timing Diagram



A1: The control supply exceeds the UV_{DBr} level. Undervoltage protection is reset.
A2: Normal operation. Switching starts at next ON transition of control input.
A3: Bootstrap supply falls below UV_{DBt}. IGBT switching is stopped.
A4: The control supply exceeds the UV_{DBr} level. Undervoltage protection is reset.
A5: Normal operation resumes. Switching starts at next ON transition of control input.

Figure 5.11 Power Supply Sequence



5.2.9 Hybrid Circuits for Control Power Supplies

Powerex provides two hybrid DC-DC converters to simplify control power supply design. The M57182N-315 and M57184N-715 are high input voltage, non-isolated, step down, DC-DC converters designed to derive low voltage control power directly from the main DC bus. These converters accept input voltages of 140VDC to 380VDC allowing them to operate directly from rectified AC line voltages of 100VAC to 240VAC. The M57182N-315 provides a 200mA regulated 15V DC output. The M57184N-715 supplies a 350mA, 15VDC output and a 200mA, 5V DC output. Each circuit is configured in a compact SIP (Single In-line Package) to allow efficient layout with minimum printed circuit board space.

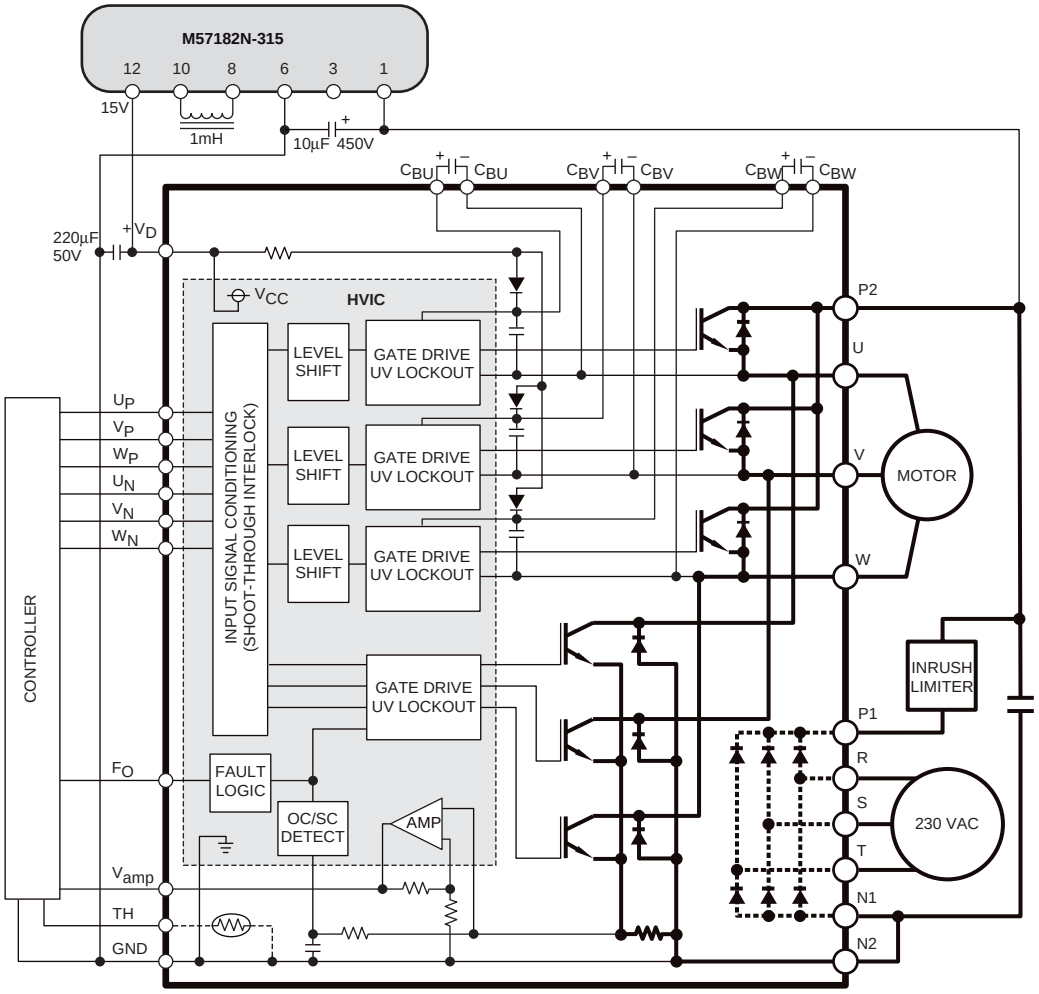
The Powerex M57184N-715 hybrid DC-DC converter is ideal for creating the 15V control power supply and the 5V logic supply directly from the DC bus. Powerex ASIPMs have integrated bootstrap circuits to provide floating power for the high-side gate drivers. These modules are designed to use a single 15V control power supply to power all of the built-in gate drive and protection circuits. Figure 5.12 shows a typical application circuit for a Powerex Version 3 ASIPM using the M57182N-315 for the 15V control power when the 5V supply is available from another source. The figure shows how the

required power supplies are derived directly from the main DC link voltage (V_{CC}). For more detailed information on the hybrid DC-DC converters see the individual device data sheets and Powerex application note “Product Information: M57182N-315 and M57184N-715 Hybrid DC-DC Converters”.

5.2.10 Ground Connection

The GND and N2 terminals are connected inside the Version 3 ASIPM. External connections between these two pins must be avoided. The GND terminal is intended to conduct only the control circuit-current. All of the main DC link current should flow in the N2 terminal. If an off-bus power supply is being used as shown in Figure 5.13, be careful not to create a ground loop by connecting the negative DC bus to the GND terminal. If the GND and N2 terminal are externally connected some of the main power circuit-current may be diverted to the GND terminal and cause voltage fluctuations that will disrupt the operation of the ASIPMs control and protection circuits.

Figure 5.12 Control Power Supply for Version 3 ASIPM



5.3 Interface Circuit

The Version 3 ASIPM has eight microprocessor compatible input and output signals. The built-in HVIC level shifters allow all signals to be referenced to the common ground of the 15V control power supply. The signals are 5V TTL/ CMOS compatible in order to permit direct connection to a PWM controller. This section presents the electrical characteristics of the ASIPM's control signal inputs and outputs, and provides detailed descriptions of typical interface circuits.

5.3.1 General Requirements

Figure 5.14 shows the internal structure of the Version 3 ASIPM control signals and a simplified schematic of a typical external interface circuit. ON and OFF operations for all six of the ASIPM's IGBTs are controlled by the active low control inputs U_P, V_P, W_P, U_N, V_N, W_N. Normally, these inputs are pulled high to the 5V logic supply of the controller with an external 5.1kΩ resistor. The controller commands the respective IGBT to turn on by pulling the input low. The pull-up resistance should be made as low as the controllers current sinking capability will allow in order to provide the best possible noise immunity. Approximately 1.6V of hysteresis is provided on all control inputs to help prevent oscillations and enhance noise immunity. The optional capacitor (C) and resistor (R), shown dashed in the figure, can be added to further improve noise filtering. These components may be required in some applications depending on the circuit layout and length of connections to the controller. If these filters are added it is important to check that proper dead time is being maintained. The control inputs should be pulled up to between 4.5V and 5.5V in the off-state. Pull up voltages larger than 6.2V are not permitted because they may disturb the ASIPM's internal reference voltage (V_{reg}).

Figure 5.13 Ground Connection

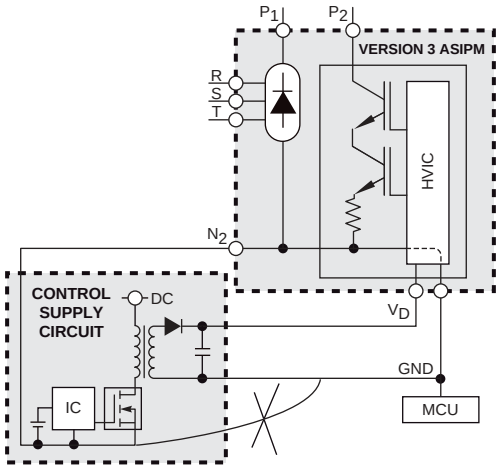
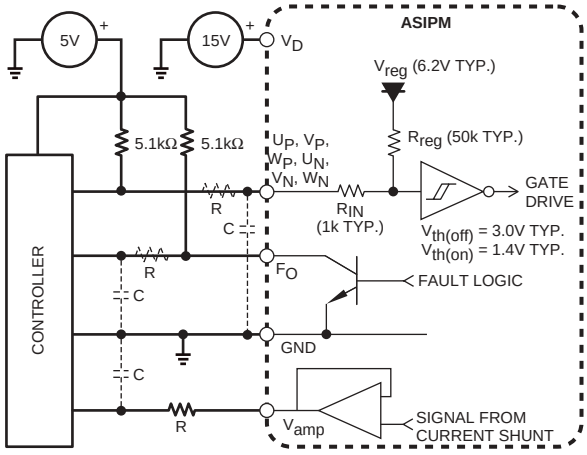


Figure 5.14 ASIPM Interface Circuit

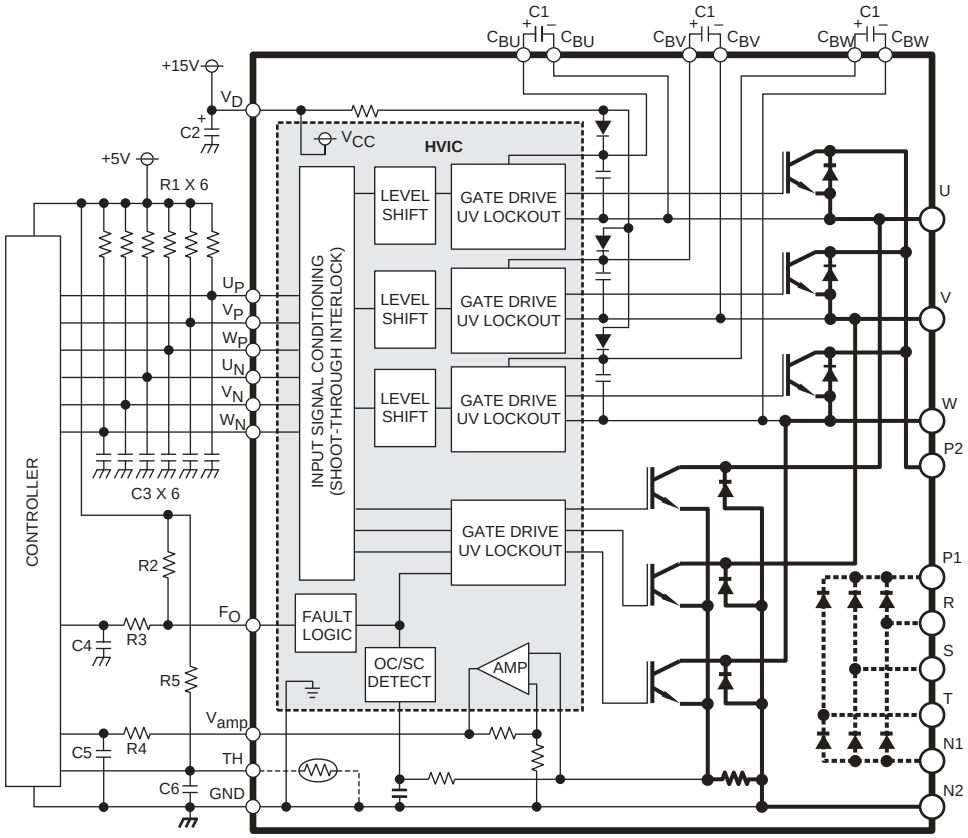


The fault signal output (F_O) is in an open collector configuration. Normally, the fault signal line is pulled high to the 5V logic supply with a 5.1kΩ resistor as shown in Figure 5.14. When an overcurrent condition or improper control power supply voltage is detected, the Version 3 ASIPM turns on the internal open collector device and pulls the fault line low. The maximum allowable sink current at the F_O pin is 15mA. The optional resistor and capacitor shown in the

fault signal connection can be added to provide noise filtering.

The buffered analog current feedback signal, V_{amp} is a zero to 5V signal proportional to the negative DC link current. The maximum output current from V_{amp} is 1mA. In many applications this signal can be connected directly to the controller's analog port. However, depending on the controller's characteristics a series resistor as shown in Figure 5.14 may be required for matching. In addition, it may be necessary to add a noise filtering capacitor.

Figure 5.15 ASIPM Complete Interface Circuit



Component Selection:

Dsgn.	Typ. Value	Description
C1	10-100µF, 50V	Bootstrap supply reservoir – Electrolytic, long life, low impedance, 105°C (Note 4)
C2	10-100µF, 50V	Control power supply filter – Electrolytic, long life, low impedance, 105°C (Note 5)
C3	100-1000pF, 50V	Input signal noise filter – Multilayer ceramic (Note 1)
C4	100-1000pF, 50V	Fault signal noise filter – Multilayer ceramic (Note 1)
C5	1000pF, 50V	Analog current feedback signal filter – Multilayer ceramic (Note 3)
C6	.22uF, 50V	Temperature sensor noise filter – Multilayer ceramic (Note 1)
R1	5.1k ohm	Control input pull-up resistor (Note 1, Note 2)
R2	5.1k ohm	Fault output signal pull-up resistor (Note 3)
R3	100 ohm-10k ohm	Fault output noise filter (Note 1)
R4	10k ohm	Analog current feedback signal filter (Note 3)
R5	10k ohm	Temperature sensor biasing resistor

Notes:
1) To prevent control signal oscillations minimize wiring length to controller (~2cm). Additional RC filtering (C3, C4, C5, C6) may be required. If filtering is added be careful to maintain proper dead-time.
2) Internal HVIC provides high voltage level shifting allowing direct connection of all six driving signals to the controller.
3) F_O output is an open collector type. This signal should be pulled high with 5.1k ohm resistor (R2).
4) Bootstrap supply capacitors must be adjusted depending on the PWM frequency and technique.
5) Local decoupling filter capacitor must be connected as close as possible to the modules pins.

5.3.2 Interface Circuit Example

Figure 5.15 shows a typical interface circuit for direct connection of the ASIPM to the PWM controller. Component selection information and relevant notes are included below the figure.

5.4 Current Sensing Function

A schematic diagram of the Version 3 ASIPM's current sensing circuit is shown in Figure 5.16. The HVIC in the Version 3 ASIPM provides a DC link current analog feedback signal through the V_{amp} terminal for system control. The signal is derived by amplifying the voltage across a built-in shunt resistor that monitors the current in the emitters of the low-side IGBTs. The buffer amplifier gain is adjusted to provide a 4V output when the peak load current reaches 200% of the modules rated inverter output current (I_O).

Figure 5.17 illustrates the performance of the feedback signal. Note that when the output current is 0A, several mV of residual voltage may exist. The typical zero current offset voltage is around 20mV. For a V_{amp} output of more than 100mV, the signal has the linear characteristics shown in Figure 5.17. The temperature dependency of the 600V and 1200V Version 3 ASIPM's V_{amp} is shown in Figures 5.18 and 5.19.

As shown in Figure 5.16, the current sensing resistor in the Version 3 ASIPM is connected so that only the current flowing in the emitters of the low-side IGBTs is detected. During normal inverter operation the current that flows in the low-side free-wheeling diodes is diverted around the current sensing resistor. There are two advantages of this configuration.

1) Sensing only the IGBT current simplifies control by making detection of output frequency, power factor and other operating conditions easier.

Figure 5.16 Current Sensing Circuit

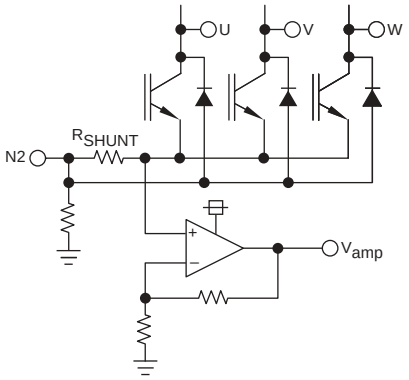


Figure 5.17 DC Link Current Analog Feedback Signal Performance

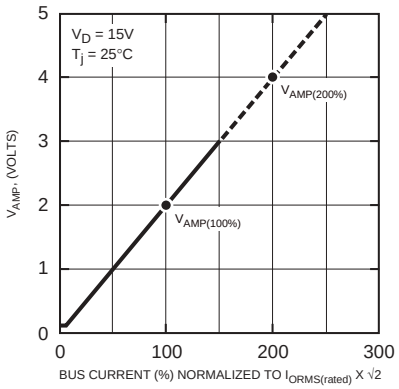


Figure 5.18 Temperature Dependency of V_{amp} for PS1103X Series

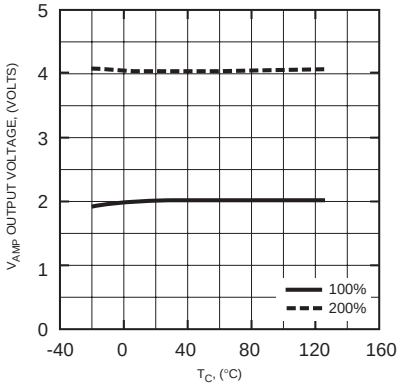
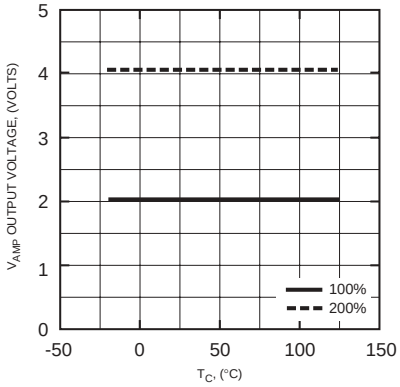


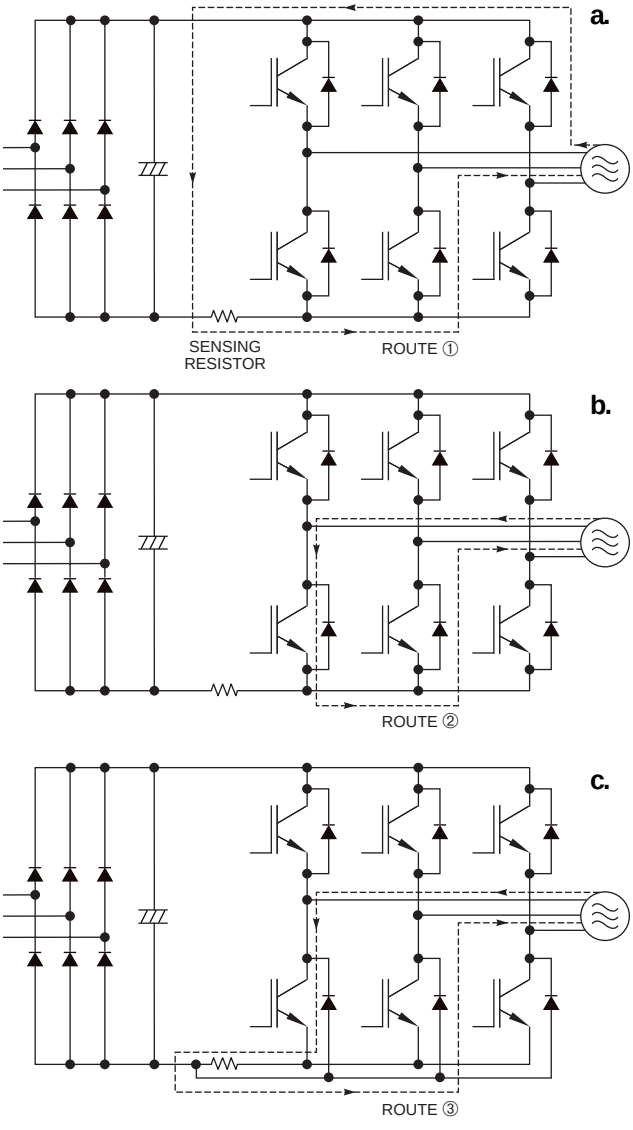
Figure 5.19 Temperature Dependency of V_{amp} for PS1203X Series



2) With this configuration it is possible to prevent damage caused by connection of the AC mains to the inverter's motor output. When an inverter is miswired in this way the DC link capacitor will be charged from the AC source as shown in Figure 5.20a. When the PWM control starts it will

normally initiate charging of the bootstrap circuits. To do this, the lower-arm IGBTs are turned on and a short-circuit condition occurs as shown in Figure 5.20b. The path of the short-circuit current misses the current shunt so this condition cannot be detected and the module will be destroyed. By separating the N-side IGBT emitters from the free-wheeling diode anode, the fault current flows through the sensing resistor as shown in Figure 5.20c. The fault condition can now be detected by the ASIPM's built-in short-circuit protection.

Figure 5.20



a. During a miswire the DC link capacitor charges through the free-wheel diodes.

b. When the PWM starts a short-circuit current flows without going through the shunt.

c. Separation of free-wheeling path allows detection of the short-circuit.

5.5 Short-circuit and Overcurrent Protection Functions

The voltage across the built-in shunt resistor is also monitored to provide protection against short-circuit and overcurrent conditions. The protection is designed to allow maximum utilization of power device capability while avoiding nuisance tripping.

Figure 5.21 shows the short-circuit and overcurrent protection circuit. The ASIPM detects the current in the N-side IGBTs. The comparator compares the detected voltage against a set reference level, V_{ref}. The RC filter adds a time delay to prevent erroneous operation of the protection due to free-wheeling diode recovery.

Figure 5.22 shows the time dependent SC and OC trip levels for the Version 3 ASIPMs. When a severe low impedance fault causes the current to exceed more than two times the IGBT's IC rating, the short-circuit protection is activated and shut-down occurs very quickly (approximately 2μs). Under less

Figure 5.21 SC and OC Protection Circuit

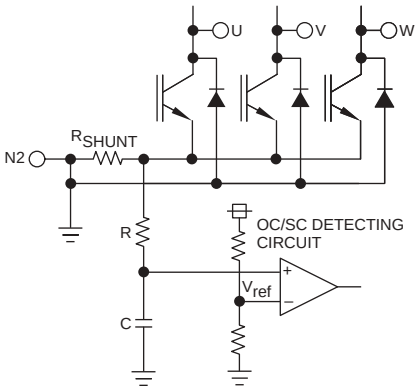
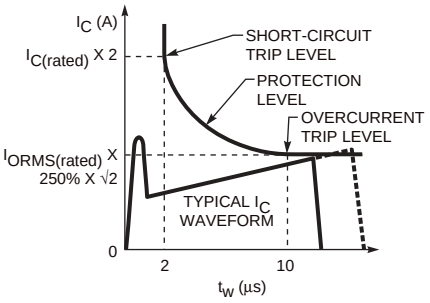


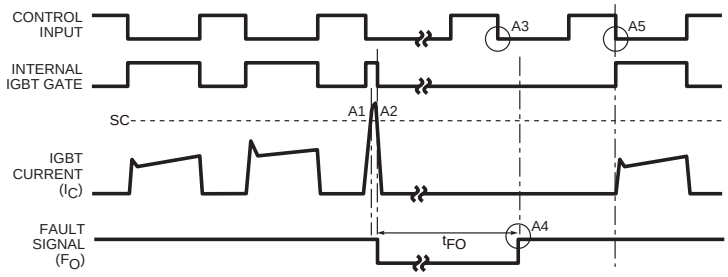
Figure 5.22 Short-circuit and Overcurrent Protection Function



severe overload conditions the trip time extends to 10µs. The overcurrent protection is set to activate when the peak current reaches a level equivalent to a load current of approximately 250% of the modules inverter current output rating (I_O).

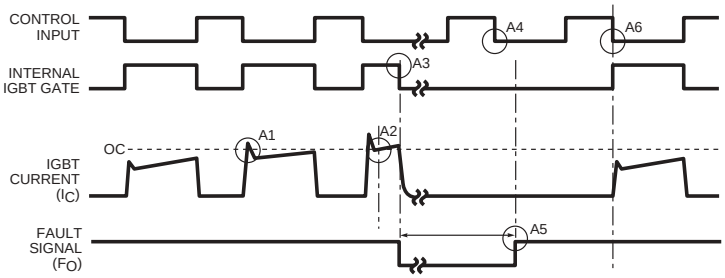
When the current exceeds the OC or SC trip level, all the low-side IGBT gates are immediately interrupted and a fault signal is generated. The IGBTs remain off until the fault time (t_{FO}) has expired and the input signal has cycled to its off- state. The duration of t_{FO} is typically a fixed 1.8ms pulse. Activation of the OC and SC protection functions indicates stress beyond the ASIPM's repetitive ratings. When an OC or SC condition is indicated, the system controller should suppress the inverter operation until the problem that caused the fault is corrected. Figures 5.23 and 5.24 show the timing diagrams of the short-circuit and overcurrent protection functions. Figures 5.25 and 5.26 represent the temperature dependency of the overcurrent trip levels.

Figure 5.23 Timing Diagram for Short-circuit Protection



A1: Current exceeds short circuit trip level.
A2: Protection activates t_{SC} after A1. Low side IGBTs are turned off. Fault signal is set.
A3: Input ON commands are ignored during t_{FO}.
A4: t_{FO} expires and fault signal is cleared.
A5: Switching of IGBT resumes at the first on going transition after the fault signal is cleared.

Figure 5.24 Timing Diagram for Overcurrent Protection



A1: Free-wheel diode recovery current pulse ignored due to t_{OC} delay.
A2: Current exceeds overcurrent trip level (OC).
A3: Protection activates t_{OC} after A2. Low side IGBTs are turned off. Fault signal is set.
A4: Input ON commands are ignored during t_{FO}.
A5: t_{FO} expires and fault signal is cleared.
A6: Switching of IGBT resumes at the first on going transition after the fault signal is cleared.

Figure 5.25 Normalized Temperature Dependency of OC Trip Level for PS1103X Series

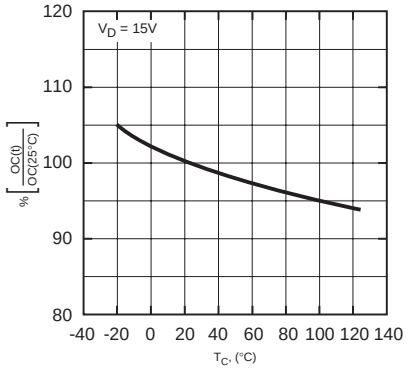
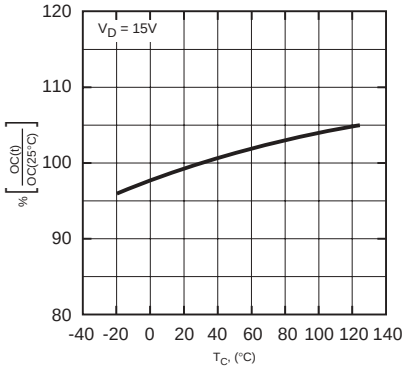


Figure 5.26 Normalized Temperature Dependency of OC Trip Level for PS1203X Series



5.6 Shoot-through Interlock Protection Function

The HVIC also provides shoot-through interlock logic for additional protection against noise and control signal anomalies. The interlock function rejects input signals that command the upper and lower IGBTs in a given leg to be on simultaneously. Operation of the interlock protection function does not produce a fault signal.

Figure 5.27 is a timing diagram showing the operation of the interlock function. If one of the arms of a given phase is on and noise is superimposed on the other arm of the phase, the interlock circuit interrupts the noise signal and the gate drive to the IGBT is blocked. If several input signals are simultaneously applied to an arm of a given phase, only the first signal is transferred to the gate drive of the corresponding IGBT. Other signals are blocked until the original IGBT is turned off.

The shoot-through interlock function is intended for protection against unexpected noise. In normal operation the CPU should provide proper dead-time.

5.7 Temperature Sensing Function

A temperature sensing function is offered on the 1200V Version 3 ASIPMs (PS1203X series). With the help of a built-in thermistor, the base plate temperature can be sensed through the TH and GND terminals. An example of a temperature-sensing interface circuit is shown in Figure 5.28. A typical resistance versus temperature characteristic for the built-in thermistor is shown in Figure 5.29. The resistance of the thermistor as a function of base plate temperature is given by:

$$R_T = R_{TO} \bullet e^{\left(\frac{\beta \bullet (T_O - T)}{T \bullet T_O}\right)} \quad (\Omega)$$

where:
T_O = reference temperature, usually 298K (25°C)
T = baseplate temperature (K)
R_T = Thermistor resistance at temperature T
R_{TO} = thermistor resistance at temperature T_O
β = thermistor material constant

NOTE: All temperatures must be in K where 0°C = 273K

The β and R_{TO} parameters are specified on the ASIPM data sheet. The above equation can also be solved for base plate temperature T. This form of the equation is shown below and is useful in cases where the resistance of the thermistor is known and the corresponding base plate temperature must be computed.

$$T = \frac{1}{\frac{1}{\beta} \bullet \ln\left(\frac{R_T}{R_{TO}}\right) + \frac{1}{T_O}} \quad (K)$$

Figure 5.28 Temperature Sensing Interface Circuit

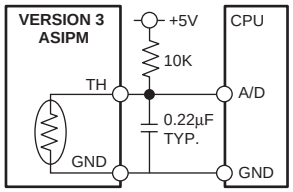


Figure 5.29 Typical Characteristic of the Built-in Thermistor

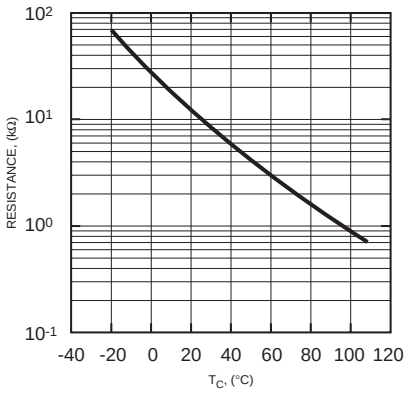
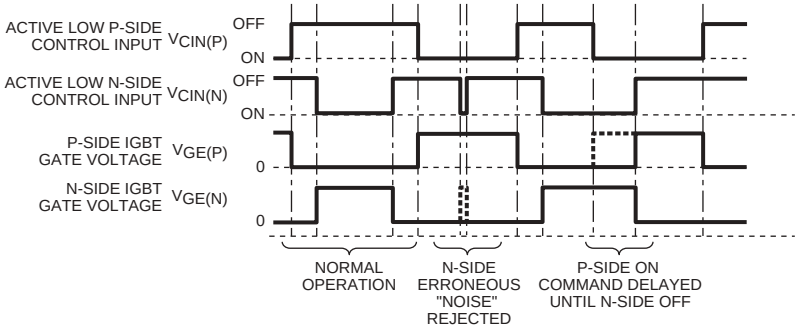


Figure 5.27 Shoot-through Interlock Timing Diagram



5.8 Fault Output

The Version 3 ASIPMs have a fault signal output for the N-side IGBTs. The fault signal is used to inform the system controller if the ASIPM's protection functions have been activated.

The fault signal output is in an active low open collector configuration. When a fault occurs the fault line pulls low and all the gates of the N-side IGBTs are interrupted. If the fault is caused by an N-side SC or OC condition, the output asserts a fixed 1.8ms pulse and is then automatically reset. In the case of an N-side control supply UV lockout fault, the signal is maintained until the control supply returns to normal.

The internal overcurrent and short-circuit protection functions are designed to protect the ASIPM from non-repetitive abnormal current. Operation of an ASIPM is guaranteed only within its maximum published ratings. Therefore, the device should not be continuously stressed above its maximum ratings. The DC-link current analog feedback (V_{amp}) should be used to regulate current within this limit. As soon as a fault output (F_O) is given from the module, the system operation should immediately shift to a proper fault clearance mode stopping all operations of the ASIPM.

5.9 Thermal Considerations

When operating, the power devices contained in Version 3 ASIPMs will have conduction and switching power losses. The heat generated as a result of these losses must be conducted away from the power chips and into the environment using a heat sink. If an appropriate thermal system is not used, then the power devices will overheat, which could result in failure. In many applications the maximum usable power output of the module will be limited by the systems thermal design.

5.9.1 Power Losses

The first step in thermal design is the estimation of total power loss. In power electronic circuits using IGBTs, the two most important sources of power dissipation that must be considered are conduction losses and switching losses.

Conduction Losses

Conduction losses are the losses that occur while the IGBT is on and conducting current. The total power dissipation during conduction is computed by multiplying the on-state saturation voltage by the on-state current. In PWM applications the conduction loss should be multiplied by the duty factor to obtain the average power dissipated. A first approximation of conduction losses can be obtained by multiplying the IGBT's rated $V_{CE(sat)}$ by the expected average device current. In most applications the actual losses will be less because $V_{CE(sat)}$ is lower than the data sheet value at currents less than rated I_C. When switching inductive loads the conduction losses for the free-wheel diode must be considered. Free-wheel diode losses can be approximated by multiplying the data sheet V_{FM} by the expected average diode current.

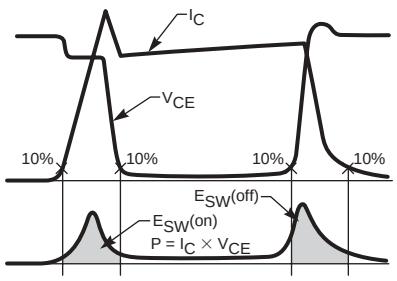
Switching Losses

Switching loss is the power dissipated during the turn-on and turn-off switching transitions. In high frequency PWM switching losses can be substantial and must be considered in thermal design.

The most accurate method of determining switching losses is to plot the I_C and V_{CE} waveforms during the switching transition. Multiply the waveforms point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy expressed in Watt-seconds/pulse or J/pulse. The area is usually computed by graphic integration. Digital oscilloscopes with waveform processing capability will greatly simplify switching loss calculations.

The standard definitions of turn-on ($E_{SW(on)}$) and turn-off ($E_{SW(off)}$) switching energy are given in Figure 5.30. The waveform shown is typical of hard switched inductive load applications such as motor drives. From Figure 5.30 it can be observed that there are pulses of power loss at turn-on and turn-off of the IGBT.

Figure 5.30 Switching Losses



The instantaneous junction temperature rise due to these pulses is not normally a concern because of their extremely short duration. However, the sum of these power losses in an application where the device is repetitively switching on and off can be significant. In cases where the operating current and applied DC bus voltage are constant and, therefore, $E_{SW(on)}$ and $E_{SW(off)}$ are the same for every turn-on and turn-off event, the average switching power loss can be computed by taking the sum of $E_{SW(on)}$ and $E_{SW(off)}$ and dividing by the switching period T. Noting that dividing by the switching period is the same as multiplying by the frequency results in the most basic equation for average switching power loss:

$$P_{SW} = f_{SW} \times (E_{SW(on)} + E_{SW(off)})$$

where:

f_{SW} is switching frequency

$E_{SW(on)}$ is turn-on switching energy

$E_{SW(off)}$ is turn-off switching energy

Switching energy curves are very useful for initial loss estimation. Figures 5.31 through 5.42 show turn-on and turn-off switching energy as a function of collector current for the PS1103X series of ASIPMs. Switching energy curves like these are also available for the PS1203X series. These curves are made using a half-bridge test circuit with an inductive load. The turn-on losses include the losses caused by the hard recovery of the opposite free-wheel diode. The critical conditions including junction temperature (T_j), DC bus voltage (V_{CC}), and control supply voltage (V_D) are given on the curves.

In applications where the operating current and applied DC bus voltage are constant the average switching power loss can be computed by reading $E_{SW(on)}$ and $E_{SW(off)}$ from the curve at the operating current and using the equation given above. In applications where the current is changing such as in a sinusoidal output inverter the loss computation becomes more complex. In these cases it is necessary to consider the change in switching energy at each switching event over a fundamental cycle.

A method for loss estimation in a sinusoidal output PWM inverter is given in Section 5.9.2. Final switching loss analysis should always be done with actual waveforms taken under worst case operating conditions. The main use of the estimated power loss calculation is to provide a starting point for preliminary device selection. The final selection must be based on rigorous power and temperature rise calculations.

5.9.2 VVVF Inverter Loss Calculation

The most common application of Version 3 ASIPMs is the variable voltage variable frequency (VVVF) inverter. In VVVF inverters, PWM modulation is used to synthesize sinusoidal output

Figure 5.31 PS11032 Switching Energy (Inverter Part P-side)

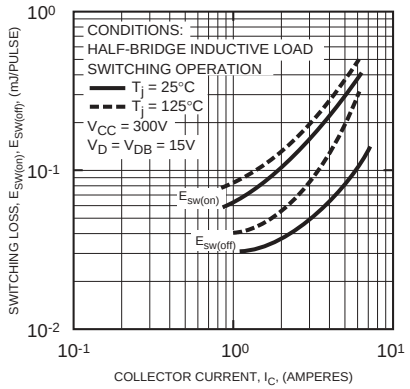


Figure 5.32 PS11032 Switching Energy (Inverter Part N-side)

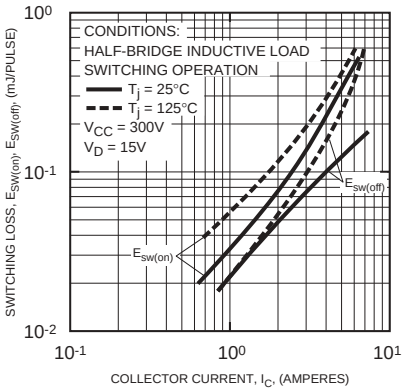


Figure 5.33 PS11033 Switching Energy (Inverter Part P-side)

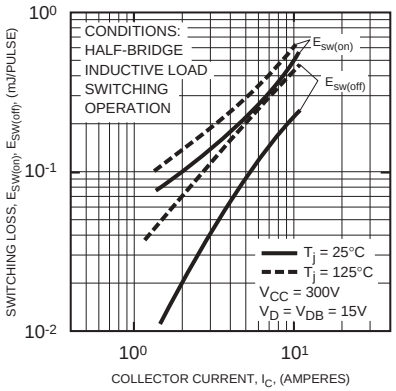


Figure 5.34 PS11033 Switching Energy (Inverter Part N-side)

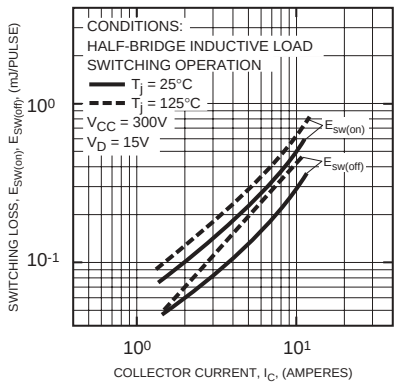


Figure 5.35 PS11034 Switching Energy (Inverter Part P-side)

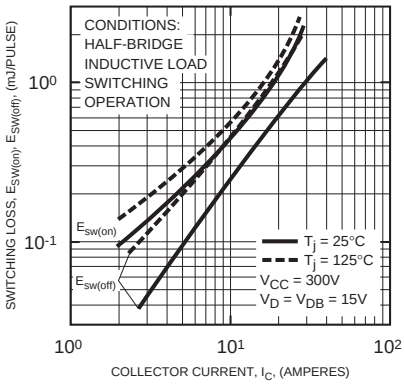


Figure 5.36 PS11034 Switching Energy (Inverter Part N-side)

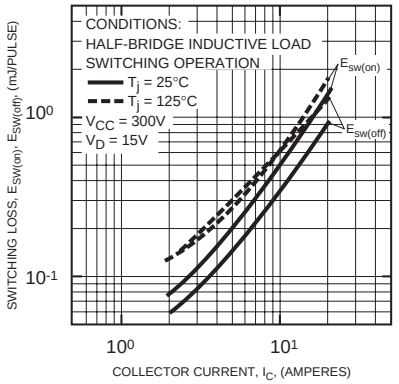


Figure 5.37 PS11035 Switching Energy (Inverter Part P-side)

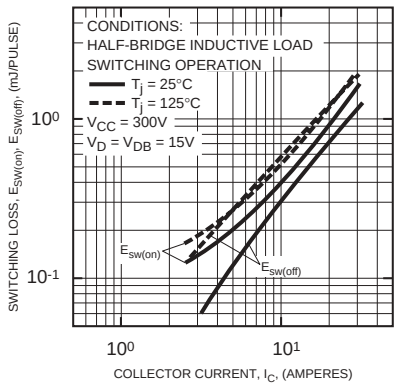


Figure 5.38 PS11035 Switching Energy (Inverter Part N-side)

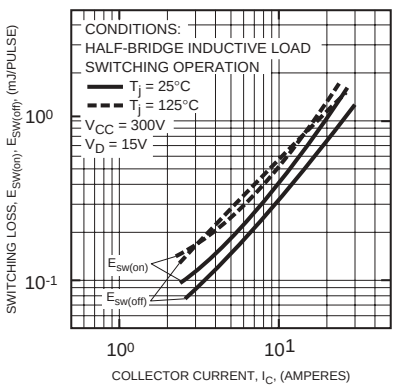


Figure 5.39 PS11036 Switching Energy (Inverter Part P-side)

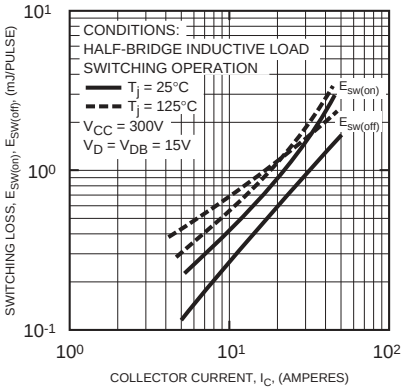


Figure 5.40 PS11036 Switching Energy (Inverter Part N-side)

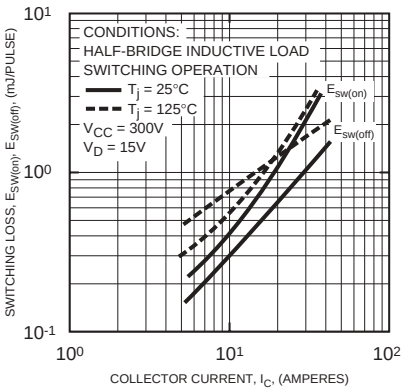


Figure 5.41 PS11037 Switching Energy (Inverter Part P-side)

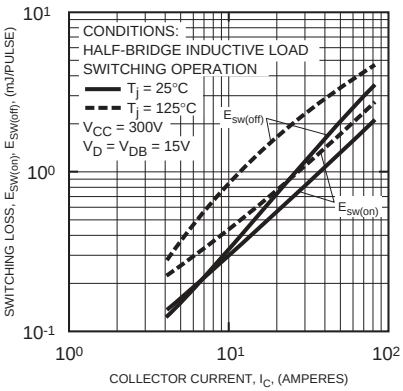
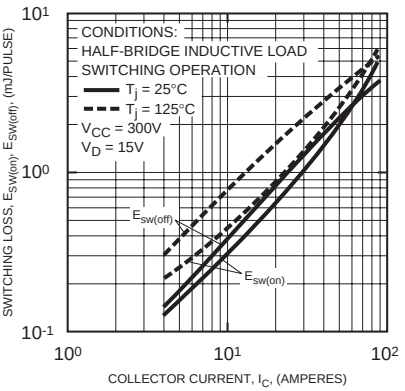
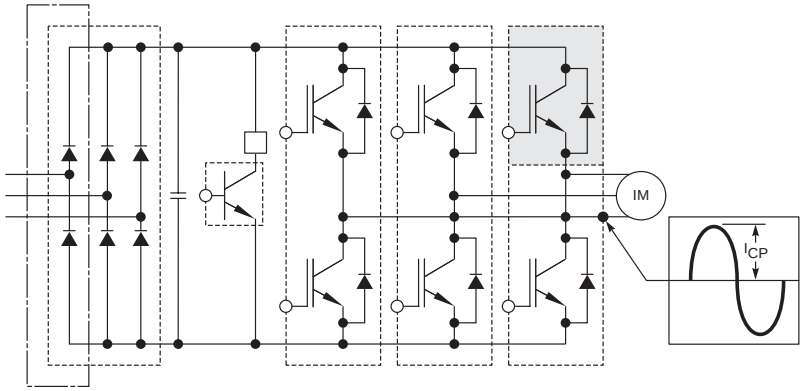


Figure 5.42 PS11037 Switching Energy (Inverter Part N-side)



currents. Figure 5.43 is a typical VVVF inverter circuit and output waveform. In this application the IGBT current and duty cycle are constantly changing making loss estimation very difficult. The following outline of equations can be used for initial loss estimation in VVVF applications. Actual losses will depend on temperature, sinusoidal output frequency, output current ripple and other factors.

Figure 5.43 Typical VVVF Inverter Circuit and Output Waveform



A. Assumptions

1. Sine waveform current output PWM control VVVF inverter
2. PWM signals generated by the comparison of sine waveform and triangular waveform.
3. Duty amplitude of PWM signals varies within the range:

$$\frac{(1-D)}{2} \Rightarrow \frac{(1+D)}{2} \quad (\%/100)$$

4. Output current is given by

$$I_{CP} \bullet \sin x$$

and it does not have ripple.

5. Load power factor for output current is cos θ. However, an ideal inductive load is assumed for switching.
6. IGBT saturation voltage $V_{CE(sat)}$ is in proportion to the collector current I_C.
7. Forward voltage drop of free-wheeling diode V_{EC} is in proportion to the forward current I_{EC}.
8. Switching losses $P_{SW(on)}$ and $P_{SW(off)}$ are in proportion to the collector current.
9. Reverse current of free-wheeling diode is constant regardless of the forward current I_{EC}.

B. Equations Derivation

For the time t, duty ratio of PWM signals is presented by

$$\frac{1 + D \times \sin t}{2}.$$

This corresponds to the change of output voltage. Thus, given the power factor cos θ indicating the relationship between output current and voltage, the expressions to calculate output current and PWM duty are as follows:

$$\text{Output Current} = I_{CP} \times \sin x$$

$$\text{PWM Duty} = \frac{1 + D \times \sin(t + \theta)}{2}$$

So, $V_{CE(sat)}$ and V_{EC}, at any point x in the fundamental output, are given specified by:

$$V_{CE(sat)} = V_{CE(sat)}(@I_{CP}) \times \sin x$$

$$V_{EC} = V_{EC}(@I_{ECP} = I_{CP})(-1) \times \sin x$$

Therefore, the average static loss of the IGBT will be:

$$\frac{1}{2\pi}\int_0^{\pi} (I_{CP} \times \sin x) \times V_{CE(sat)}(@I_{CP}) \times \frac{1 + D\sin(x+\theta)}{2} \bullet dx$$

$$= I_{CP} \times V_{CE(sat)}(@I_{CP}) \times \frac{1}{2\pi}\int_0^{\pi} (I_{CP} \times \sin^2 x) \times \frac{1 + D\sin(x+\theta)}{2} \bullet dx$$

$$= I_{CP} \times V_{CE(sat)}(@I_{CP}) \times \left[\frac{1}{8} + \frac{D}{3\pi}\cos\theta\right]$$

Similarly, the static loss of free-wheeling diode is:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} [(-1) \times I_{CP} \times \sin x] \times [(-1) \times V_{EC}(@I_{CP}) \times \sin x] \times \frac{1 + D\sin(x+\theta)}{2} \bullet dx$$

$$= I_{CP} \times V_{EC}(@I_{CP}) \times \left(\frac{1}{8} - \frac{D}{3\pi}\cos\theta\right)$$

The dynamic loss of the transistor does not depend on PWM duty and is given by:

$$\frac{1}{2\pi}\int_0^{\pi}[E_{SW(on)}(@I_{CP}) + E_{SW(off)}(@I_{CP}) \times \sin x] \times f_c \bullet d\chi$$

$$= [E_{SW(on)}(@I_{CP}) + E_{SW(off)}(@I_{CP})] \times f_c \times \frac{1}{\pi}$$

The dynamic loss in the free-wheeling diode can be approximated assuming the idealized waveform shown in Figure 5.44. Graphical integration of this waveform yields:

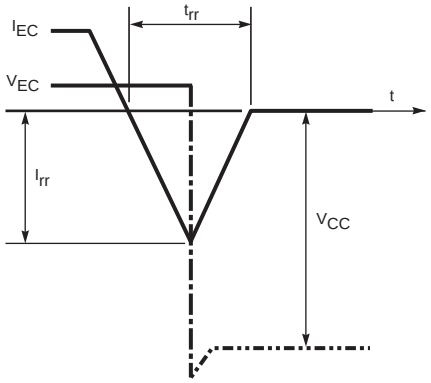
$$E_{SW} = \frac{I_{RR} \times V_{CC} \times t_{RR}}{4} \text{ (const.)}$$

As a result, the total power loss due to free-wheel diode recovery is given by:

$$\frac{I_{RR} \times V_{CC} \times t_{RR}}{4} \times f_c \frac{1}{2}$$

$$\frac{1}{8} \times (I_{RR} \times V_{CC} \times t_{RR} \times f_c)$$

Figure 5.44 FWDi Dynamic Loss



C. Summary of Equations

1. Static Loss of IGBT

$$I_{CP} \times V_{CE(sat)}(@I_{CP}) \times \left(\frac{1}{8} + \frac{D}{3\pi}\cos\theta\right)$$

2. Dynamic Loss of IGBT

$$(E_{SW(on)} + E_{SW(off)}) \times f_c \times \frac{1}{\pi}$$

3. Static Loss of Free-wheeling Diode

$$I_{ECP} \times V_{EC}(@I_{FP} = I_{CP}) \times \left(\frac{1}{8} - \frac{D}{3\pi}\cos\theta\right)$$

4. Dynamic Loss of Free-wheeling Diode

$$\frac{1}{8} \times (I_{RR} \times V_{CC} \times t_{RR} \times f_c)$$

Symbology:

$E_{SW(on)}$: IGBT's turn-on switching energy per pulse at peak current, I_{CP} and T = 125°C

$E_{SW(off)}$: IGBT's turn-off switching energy per pulse at peak current, I_{CP} and T = 125°C

f_{SW}: PWM switching frequency for every inverter arm-switch (normally, $f_{SW} = f_c$)

I_{CP}: Peak value of sinusoidal output current ($I_{CP} = I_{EP}$)

$V_{CE(sat)}$: IGBT saturation voltage drop @ I_{CP} and T = 125°C

V_{EC}: FWDi forward voltage drop @ I_{EP}

D: PWM duty factor (modulation depth)

q: Phase angle between output voltage and current

I_{rr}: Diode peak recovery current

t_{rr}: Diode reverse recovery time

$V_{CE(pk)}$: Peak voltage across the diode at recovery

When using these equations, it is important to keep in mind that the actual losses depend on the details of the PWM technique. The relationship between PWM duty and output current will also depend on the characteristics of the load. The losses calculated using these equations must be verified by measurement in the actual application. The E_{SW}, $V_{CE(sat)}$ and V_{EC} values should be taken from T_j = 125°C data.

5.10 Protection Against Noise

The noise withstand capability of the Version 3 ASIPMs varies greatly with each application. It depends on the wiring patterns, parts layout and other factors in each system. We therefore recommend that a noise test be performed on the actual finished system.

There are noise countermeasures implemented within the Version 3 ASIPMs. They achieve improved noise withstand capability through optimized internal wiring to reduce inductance and optimized isolation to reduce leakage current to the heat sink.

There are also noise countermeasures that can be executed outside of the Version 3 ASIPMs. They are as follows.

Control input:

- Improving power supply filtering (close to ASIPM terminals)
- Lowering impedance at control inputs (reducing pull-up resistance)
- Adding RC filter on the control inputs
- Reduce length of wiring on control inputs

AC input line:

- To guard against common-mode dV/dt noise at the AC input line, connect a surge absorber and a high frequency type filter capacitor (2.2nF ~ 6.5nF) across each input line (R,S,T) and the system earth ground.

Output:

- To guard against noise from the inverter output line (e.g. by mechanical contactor action, due to long cabling, etc.), connect an AC filter at each output.

6.0 Handling Notice

Handling precautions

A. Transportation

(1) Boxes must be stored and shipped in the proper orientation to avoid deformation of module pins.

(2) Do not drop packages or subject them to excessive shock

(3) Avoid contact with water. Do not allow boxes to be exposed to rain or snow.

B. Storage

(1) Modules should be stored at normal room temperature and humidity: 20°F to 95°F (5°C to 35°C) and 45% to 75% relative humidity. Long-term storage at conditions significantly different from these may cause quality and/or reliability problems.

(2) Modules must be kept dry

(3) Modules must not be exposed to organic solvents, corrosive gasses, flammable gasses, fine dust or salt

(4) If stored for an extended period modules should be carefully inspected for signs of corrosion or degradation of exterior surfaces

C. ESD

(1) Control IC's used in the Version 3 ASIPMs have MOS gate structure and must be handled using all appropriate ESD safe procedures.

(2) Avoid all potential sources of ESD including human contact and non-conductive packaging materials.

(3) Avoid touching the modules terminals with bare hands.

(4) Use static safe work areas. Conductive work surfaces and flooring and grounded wrist straps are required when handling modules with exposed pins.

(5) All machinery including soldering irons that may come in contact with the modules pins should be grounded.

(6) Never apply voltage to a module with the control pins open.